STUDENTMAP

VTU B.E/B.TECH QUESTION PAPER SET

CBCS
SEMESTER VI

DIGITAL SYSTEM DESIGN USING VERILOG

Use bookmarks to easily navigate between question papers

CBCS SCHEME

USN | | | | | | | | | | |

15EC663

Sixth Semester B.E. Degree Examination, June/July 2018
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. What are the two sources of power consumption in digital components? Explain. **(04 Marks)**

b. Develop a verilog model for a 4 : 1 multiplexer. **(04 Marks)**

c. Design an encoder for the buglar alarm that has sensors for each of the 8 zones as a priority encoder with zone 1 having highest priority down to zone 8 having lowest priority. **(08 Marks)**

OR

2 a. Explain the simple design methodology followed in IC industry. **(08 Marks)**

b. Develop a datapath to perform complex multiplication of two complex number whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post-binary points. Real and imaginary parts of the product are represented with 8 pre-binary points and 24 post-binary points. Area is the main constraint. Also write the verilog model of the complex multiplier datapath. **(08 Marks)**

Module-2

3 a. Design a $1m \times 8$ bit composite memory using 512 K $\times 8$ bit memory component. **(04 Marks)**

b. Design a $16K \times 48$ – bit memory using $16K \times 16$ – bit memory component. **(04 Marks)**

c. Explain flowthrough and pipelined SSRAM with the help of timing diagram. **(08 Marks)**

OR

4 a. Determine whether there is an error in the ECC word 000111000100 and if so, correct it. **(06 Marks)**

b. Develop a verilog model of a dual – port $4K \times 16$ bit flow through SSRAM One port allows data to be written and read, while the other port allows data to be read. **(06 Marks)**

c. Explain dynamic RAM operation. **(04 Marks)**

Module-3

5 a. Write and explain the internal organization of a CPLD. **(08 Marks)**

b. What are the two main design and manufacturing techniques for ASIC's. Explain. **(08 Marks)**

OR

6 a. Write and explain the internal organization of FPGA. **(08 Marks)**

b. Explain differential signaling in detail. **(08 Marks)**

Module-4

7 a. Explain Flash ADC and successive approximation ADC with the help of necessary diagrams. **(08 Marks)**

b. Design an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the I/P value changes. The controller is the only interrupt source in the system. Also develop a verilog model of the I/P controller. **(08 Marks)**

OR

8 a. Explain the following serial interface standards for connecting I/O devices:
(i) I^2C (ii) USB **(08 Marks)**

b. With a neat diagram, explain R-string DAC and R/2R ladder DAC. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Explain floorplan, placement and routing of ASIC physical design. **(06 Marks)**

OR

10 a. Explain Built-In Self Test (BIST) techniques. **(08 Marks)**

b. Explain the terms scan design and boundary scan. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, June/July 2019
Digital System Design using Virology

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Define the terms setup time, hold time and clock to output time of a flip-flop and what are the constraints imposed by these parameter on the circuit operations. **(05 Marks)**

b. Develop veriology module for 7 segment decoder. Include an additional input 'blank' that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. Explain functional verification and formal verification for a verilog module **(05 Marks)**

OR

2 a. What are the effects of capacitive loading and propagation delay on signal transitions between logic levels? **(08 Marks)**

b. Develop verilog module for 4 : 1 MUX. **(04 Marks)**

c. Explain general view of digital system with data path control section. **(04 Marks)**

Module-2

3 a. Design a 64k ×8 bit composite memory using four 16k × 8 bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. **(08 Marks)**

b. Explain asynchronous static RAM with timing diagrams. **(08 Marks)**

OR

4 a. Write a note on multiport memories. **(08 Marks)**

b. Explain error detection and correction with one example. **(08 Marks)**

Module-3

5 a. Explain different types of PCB design. **(05 Marks)**

b. Explain implementation fabrics for digital system based on integrated circuit. **(07 Marks)**

c. What are EMI and cross talk? **(04 Marks)**

OR

6 a. Briefly explain programmable array logic. **(08 Marks)**

b. Explain signal integrity issue in PCB design and also explain measures to reduce these issues. **(08 Marks)**

Module-4

7 a. Explain the serial transmission of 64 bit data within clock domain with timing diagram. (08 Marks)

b. Explain the following serial interface standards for connecting I/O devices.
i) RS232 ii) Fire wire. (08 Marks)

OR

8 a. Explain any 4 analog sensors. (08 Marks)

b. Explain the concept of multiplexed buses (08 Marks)

Module-5

9 a. Explain logical partitioning and physical partitioning of a transport monitoring system. (08 Marks)

b. Explain fault model and fault simulation. (08 Marks)

OR

10 a. Explain 4 bit LFSR and CFSR for generating pseudorandom test vectors. (08 Marks)

b. Explain briefly area, power and timing optimization in digital circuits. (08 Marks)

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the following constraints imposed in real world circuits : (i) Noise margin (ii) Static levels (iii) Propagation delay (iv) Static and dynamic power consumption. **(08 Marks)**

b. Explain with illustration a simple methodology followed in IC industries. **(08 Marks)**

OR

2 a. Develop a verilog model for a 7 segment decoder. **(05 Marks)**

b. Develop a verilog model of a debouncer for a push button switch that uses a debouncer interval of 10 mS. Assume the system clock frequency is 50 MHz. **(05 Marks)**

c. Write a brief notes on finite state machine. **(06 Marks)**

Module-2

3 a. Design a 64 K * 8 bit composite memory using four 16 K×8 bit components. **(06 Marks)**

b. Explain the different ROM's used in digital system. **(06 Marks)**

c. Compute the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

OR

4 a. Explain briefly about asynchronous static RAM. **(08 Marks)**

b. Develop a verilog model of a dual port, 4K ×16bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(05 Marks)**

c. Write a note on DRAM. **(03 Marks)**

Module-3

5 a. Explain briefly about the sequence of steps involved in IC manufacture. **(06 Marks)**

b. What are the distinguishes between a plat form FPGA from a simple FPGA? **(06 Marks)**

c. Explain the differential signaling. **(04 Marks)**

OR

6 a. Write a note on complex PLDs. **(08 Marks)**

b. Explain briefly about the internal organization of an FPGA with a neat diagram. **(08 Marks)**

Module-4

7 a. Explain the analog inputs used in input devices. **(04 Marks)**

b. Explain any four serial interface standards. **(08 Marks)**

c. Explain briefly the tristate buses and weak keepers. **(04 Marks)**

OR

8 a. Design and develop the verilog code for an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. **(08 Marks)**

b. Show how 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

Module-5

9 a. Explain the hardware and software co design flow. **(08 Marks)**

b. Explain the design optimization that are must to meet the design constraints. **(08 Marks)**

OR

10 Write a short notes on :

a. Scan design and boundary scan. **(08 Marks)**

b. Built-In Self Test (BIST) **(08 Marks)**

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USN | | | | | | | | | | |

15EC663

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Develop a verilog model that expresses the logical structure of the gate circuit for vat buzzer. Assume that the sensor signals and the switch signal are inputs to the model, and that the buzzer signal is the output from the model. **(04 Marks)**

b. Develop a verilog model for a 7-segment decoder. Include an additional input, blank that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. Develop a data path to perform a complex multiplication of two complex numbers. Whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post – binary points real and imaginary parts of the product are represented with 8 pre–binary points and 24 post-binary points. Area is the main constraint. **(06 Marks)**

OR

2 a. Explain design methodology followed in IC industry with neat sketch. **(06 Marks)**

b. Develop a test bench model for the traffic light controller. Verify the conditions that, when the enable input is 1, the output is the same as the light input and when the enable input is '0' all light outputs are inactive. **(04 Marks)**

c. Write a verilog code for finite state machine of complex multiple control sequence. **(06 Marks)**

Module-2

3 a. Design 1M × 8 bit composite memory using 512 k × 8 bit memory component. **(04 Marks)**

b. Determine whether there is an error in the ECC word 000111000100 and if so correct it. **(06 Marks)**

c. Develop a verilog model of a dual–port, 4K × 16 bit flow through SSRAM. One port allows data to be written and read. While the other port only allows data to be read. **(06 Marks)**

OR

4 a. Design a 64k × 16 bit composite memory using 16K × 8 bit component. **(06 Marks)**

b. Computer the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

c. Design a FIFO to store upto 256 data items of 16 bits each, using a 256 × 16 bit dual-port SSRAM for the data storage. The FIFO should provide status outputs, to indicate, when the FIFO is empty and full. Assume that the FIFO will not be read when it is empty, nor be written to when it is full, and that the write and read ports share a common clock. **(06 Marks)**

Module-3

5 a. Outline with a neat sketch, the internal organization of a CPLD. **(06 Marks)**

b. Design 4-digit decimal counter with seven segment LED display with neat sketch using 74LS390 dual decade counter, four 74LS47 BCD to seven segment decoder, four 7-segment display, plus any additional gates required. **(10 Marks)**

OR

6 a. Outline and explain the internal organization of FPGA. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise? **(08 Marks)**

Module-4

7 a. Construct flash ADC and successive approximation ADC with a help of necessary diagram. **(08 Marks)**

b. Show how a 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

OR

8 a. With a net diagram explain R-string DAC and R/2R ladder DAC. **(08 Marks)**

b. Develop a controller for the keypad matrix and show how to connect the controller to a Gumnut core. Use output port address 4 for the matrix row output register and input address 4 for the matrix column input register. Write the verilog definition for the controller. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(08 Marks)**

b. Outline the term scan design and boundary scan with neat sketch. **(08 Marks)**

OR

10 a. Demonstrate Built-In Self Test (BIST) techniques. **(08 Marks)**

b. Illustrate the term design optimization with respect to area, timing and power. **(08 Marks)**

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