Syllabus

BASIC ELECTRONICS

Subject Code : 15ELN15/25 IA Marks : 20

Hrs/Week : 04 Exam Hrs. : 03

Total Hrs. : 50 Exam Marks : 80

MODULE 1:

Semiconductor Diodes and Applications: 6Hrs

PN Junction diode,Characteristics and Parameters,Ideal Diode, Diode Approximations.DC load line analysis,Rectification: Half-wave Rectification: Ripple factor, Power Conversion Efficiency, Full-wave Rectification: Ripple factor, Power Conversion Efficiency, Bridge Rectifier and Rectifier with Centre-Tapped (CT) Transformer,Capacitor filter circuit(only qualitative approach),Zener diode voltage regulators: Regulator circuit with no load,loaded regulator, Numerical examples as applicable .

Bipolar Junction Transistor: 4Hrs

BJT Construction and Operation: BJT Voltages and currents,BJT amplification,BJT Configurations and Characteristics: Common Base(CB) Configuration, Common Emitter (CE) Configuration Common Collector Characteristics,Numerical examples as applicable .

MODULE 2:

BJT Biasing: 4Hrs

DC Biasing: DC Load line and Bias point,Base bias, Voltage-Divider Bias, Analysis Equation, Numerical Examples as applicable.

Introduction to Operational amplifiers :6 Hrs.

Introduction, OP-AMP Architecture, Differential Amplifier. Basic OP-AMP Circuits: Inverting Amplifier, Virtual Ground, Non-inverting Amplifier.Linear Applications of OP-AMP: Summer Circuit, Subtractor.,Integrator and Differentiator, Numerical Examples.

MODULE3 :

Digital Electronics :10 Hrs.

Introduction. Switching and Logic Levels. Digital Waveform. Number Systems: Decimal \Number System, Binary Number System, Converting Decimal to Binary, Hexadecimal Number System: Converting Binary to Hexadecimal, Hexadecimal to Binary, Converting Hexadecimal to

Decimal, Converting Decimal to Hexadecimal, Octal Numbers: Binary to Octal Conversion.Complement of Binary Numbers. Boolean Algebra Theorems , De Morgan's theorem. Digital Circuits: Logic gates, NOT Gate, AND Gate, OR Gate , XOR Gate, NAND Gate, NOR Gate, X-NOR Gate. Boolean Relations (Section 11.6) Algebraic Simplification (Section 11.7) NAND and NOR Implementation ((Section 11.8): NAND Implementation, NOR Implementation. Half adder, Fulladder.

MODULE 4:

Flip-Flops :4Hrs

Introduction to Flip-Flops (Section 12.1), NAND Gate Latch/ NOR Gate Latch (Section 12.3), RS Flip-Flop(Section 12.4), Gated Flip-Flops: Clock ed RS Flip-Flop (Section 12.5).

Microcontrollers: 5Hrs

Introduction to Microcontrollers,8051 Microcontroller Architecture, Working of Microcontroller. d example of microcontroller based stepper motor control system(only block diagram approach).

MODULE 4:

Communication systems: 6 Hrs.

Introduction, Elements of Communication Systems, Modulation: Amplitude Modulation,Spectrum Power, AM Detection (Demodulation), Frequency and Phase Modulation. Amplitude and Frequency Modulation: A comparison.

Transducers : 4 Hrs.

Introduction, Passive Electrical Transducers, Resistive Transducers, Resistance Thermometers, Thermistor. Linear Variable Differential Transformer (LVDT). Active Electrical Transducers, Piezoelectric Transducer, Photoelectric Transducer

TEXT BOOKS:

1.David Bell, Electronic Devices and Circuits: OxfordUniversity Press, 5thEDn., 2008.

2.D.P. Kothari, I.J.Nagrath, Basic Electronics : McGraw Hill Education(India)Private Limited

2014

Reference Books:

1.Muhammad Ali Mazidi, The 8051 Microcontroller and Embedded. Systems. Using Assembly and C. Second Edition, 2011.

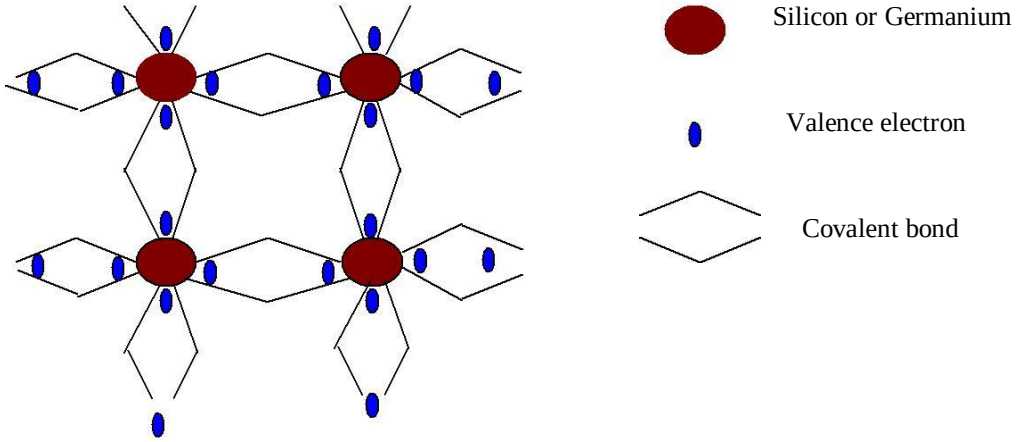
INDEX SHEET

Module 1
Semiconductor Diodes and Applications

Introduction :

The conductivity is proportional to the concentration of free electron 'n'.For a good conductor n should be very large of the order of 10^{28} electrons /cubic meter, for insulators it is 10^{7} electrons/cu. meter and for semiconductors it is in between these limits.

We know that Germanium and Silicon are the most important semiconductor semi-conductor material, used in the fabrication of electronic devices. An insight into these material is essential for proper understanding of device functioning. The crystalline structure of these materials consists of tetrahedron form, and regularly repeated through out the material having atoms on the vertex of each tetrahedron. In two dimensions this can be written as shown in the figure below.



We notice here that the valence electrons are bound to the atom in the form of a covalent bond, leaving no electrons for conduction and hence the material has poor conductivity. In order to establish the conduction this situation has to be disturbed. by the addition of impurities into the material.

Donor and acceptor impurities.

When impurity atoms are added, these atoms will displace some of the semiconductor atoms in the crystal lattice. The covalent bond gets disturbed and a new distribution of the crystalline structure takes place depending on the valence electron contained in the impurity atom.

Donor impurity

The donor impurity contains 5 valence electrons, hence when added as impurity, one electron will become free to move around with other four forming covalent bond with the neighboring atoms. This material is called donor as it donates one electron. It is also called pentavalent impurity because it contains 5 valence electrons.

The examples for pentavalent impurities are ***Antimony, Phosphorous and Arsenic***.
Addition of donor impurity increases the free electron concentration.The excess electron further nullifies the holes, which are less in number by recombining and hence the semiconductor after doping with donor impurity is called **n-type** semiconductor.

Acceptor impurities

A similar situation happens when an impurity atom with three valence electrons are added but yielding a different situation. The impurity atoms get distributed throughout the lattice structure altering the covalent bond as shown in figure below.The absence of electrons in one of the covalent bond contributes a hole and becomes a positive charge carrier. So the hole formation is the result of adding impurities having three valence electrons and are called trivalent impurity. The trivalent impurity is also called acceptor because it accepts electrons from the crystal lattice. These impurities are consequently known as acceptor or p-type impurities as they result in excess holes. Hence when acceptor impurities are added to the semiconductor it becomes **p-type,** and have holes as majority carriers for conduction. These holes dominate electrons which are minority. The acceptor impurities are ***Boron, Gallium and indium.*** The effect of adding impurity can be realized by noting the fact that when one atom of impurity is added to every 10^8 atoms of Germanium, the conductivity changes by 12 times.

n-type semiconductor

In n-type semiconductor the conduction is due to electrons, hence electrons are called majority carriers and holes are called minority carriers. Since the donor atom donates an electron it becomes positive ion. This is shown in figure 1.1 below.

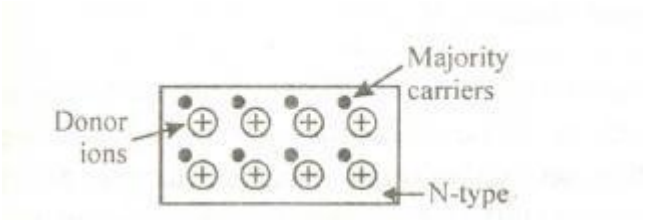


Fig1.1 : n-type semiconductor

The n-type has mobile free electrons indicated by small filled circles and the same number of

donor ions indicated by a circled positive charge.

p-type semiconductor

In p-type semiconductor, current conduction is due to excess holes and holes are called *majority* carriers and electrons are called *minority* carriers and is shown in figure 1.2.

. Since an acceptor impurity has accepted an electron it becomes negative ion. The p-type has mobile holes, and is indicated by unfilled circles and the same number of fixed negative acceptor ions indicated by an encircled negative ion The p-type has mobile holes, and is indicated by unfilled circles and the same number of fixed negative acceptor ions indicated by an encircled negative ion.

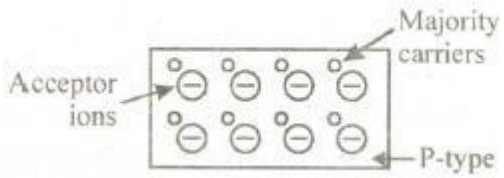


Fig 1.2 : p-type semiconductor

PN- junction

Semiconductor pn-junction is formed when a single crystal of semiconductor is added with an acceptor impurity on one side and donor impurity on the other side and is shown in figure1.3 below.In actual practice a small quantity of trivalent impurity is placed on n-type silicon material and then it is heated to a high temperature in a quartz pipe to allow diffusion of the impurity atoms into silicon. This process is known as diffusion. The other method of forming a junction is grown junction and alloying (used for Germanium semiconductor).

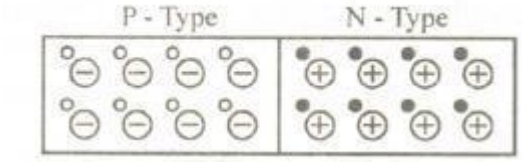


Fig1.3 : PN- junction

The figure shows a pn junction. The left side material is a p-type semiconductor having acceptor ions and positively charged holes, the right material is n-type having positive donor ions and free electrons. Since n-type has high concentration of electrons and p-type has high concentration of holes and there exists a concentration gradient across the junction. Due to this, charge carriers move from high concentration area towards low concentration area to achieve uniform distribution of charge.This is shown in figure 1.4.

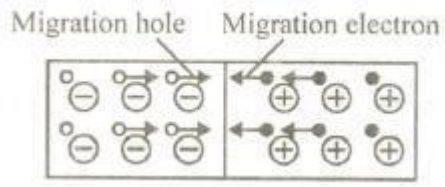


Fig 1.4: Charge distribution in PN- junction

In p-type excess holes move towards n-side similarly electrons from n-side move towards p-side, this process is called **diffusion** and diffusion of charge carriers take place on either side of the junction.This diffusion of charge carriers takes place in neighborhood of the junction immediately after the junction is formed, and the *rest of the material will be at equilibrium under no bias condition.* This is shown in figure 1.5.

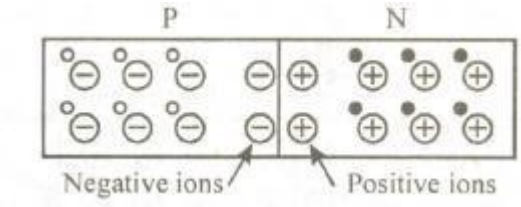


Fig 1.5.: Depletion region formation

When the migrating electrons diffuse into p-type and recombines with the acceptor atoms on p-side, the acceptor ions accepts this additional electrons and becomes negatively charged immobile ions, and the hole disappears and free electron becomes valence electron. Similarly when hole diffuses into n-side they recombine with donor atom, this donor atom accepts additional hole and they become positively charged immobile ion and electron disappears. These ions are covalent bonded and hence cannot move around freely.

After diffusion, negative ions are formed on the p-side and positive ions are formed on the n-side closer to the junction as shown in figure below. If the doping density is same on both sides then large positive charge gets accumulated on n-side and large negative charge gets accumulated on p-side of the junction, thus these charges at junction repel and do not allow further migration of carriers from one side to the other side of the junction.

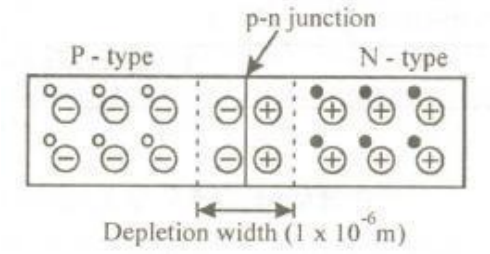


Fig1.6: Depletion region

Thus the uncovered ion in the neighborhood of the junction is depleted of mobile charges and is called **depletion region**, the **space charge region** or the **transition region.** The thickness of this region is of the order of 1micron (one millionth of a meter).

Study of pn-junction under following conditions:

a) No bias, b) Forward bias, c) Reverse bias

Biasing: Biasing is *connecting a p-n junction to an external d.c. voltage.* a) No bias condition

no bias condition is already explained above and the other conditions are discussed below.

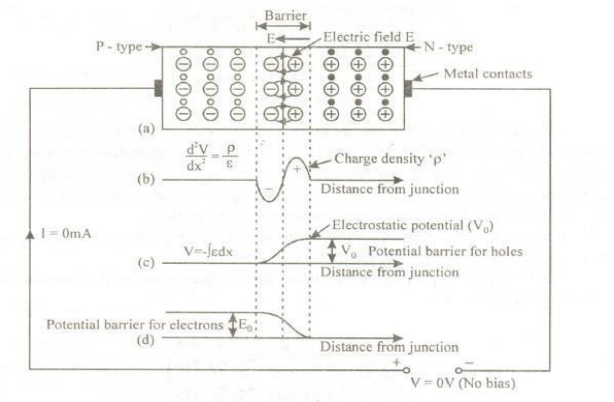


Fig **:** A pn junction under no-bias condition.

Under no bias condition, the positive charge on n-side repel the holes to cross from p ton side, negative charge on p-side repel free electrons to enter from n to p side. Thus, a barrier is setup against further movement of charge carriers, this is called potential barrier or junction barrier. The potential barrier is of the order ofO.6V for silicon and O.2V for germanium. The form of the potential energy barrier against flow of electrons from the n-side across the junction is shown in fig, since the potential barrier of electron' is inverted compared to potential barrier of holes in fig. this is due to the charge on an electron is negative. Similarly the potential barrier against flow of holes from p-side across the junction is as shown in figure 6c, and the potential is positivedue to charge on hole is positive.

Since the electrostatic potential is the negative integral ofthe function *'E:'* (electric field intensity), this variation constitute the potential barrier against further diffusion of holes and electrons. Due to the presence of potential barrier (cut-in voltage) which in turn prevents further movement ofmajority carriers across the junction. But the barrier promotes the minority carriers in n-type (holes) that finds a path to pass directly into p-type material, due to negative potential in the p-type near the junction. Similarly the minority carriers (electrons) in p-side pass directly

into n-type due to positive potential in n-type. Thus in the absence of an applied bias the net flow of charge in anyone direction for a semiconductor is zero.

b) Forward bias: The forward bias condition is shown in figure 1.8 .The condition under forward bias is explained below.

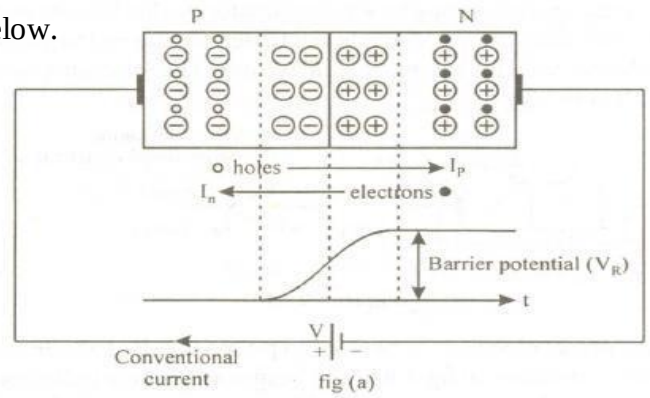


Fig.1.8 Forward biasing of p-n junction

- When an external voltage is applied to the junction, is in such a direction that it cancels the potential barrier, thus permitting current flow, is called forward biasing

- To apply forward bias, connect +ve terminal of the battery to p-type and –ve terminal to n-type as shown in fig1.8 below.
- The applied forward potential establishes the electric field which acts against the field due to potential barrier. Therefore the resultant field is weakened and the barrier height is reduced at the junction as shown in fig1.8.
- Since the potential barrier voltage is very small, a small forward voltage is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore current flows in the circuit. This is called forward current.

c) Reverse biasing : The reverse bias condition is shown in figure 1.9.The condition under reverse bias is explained below.

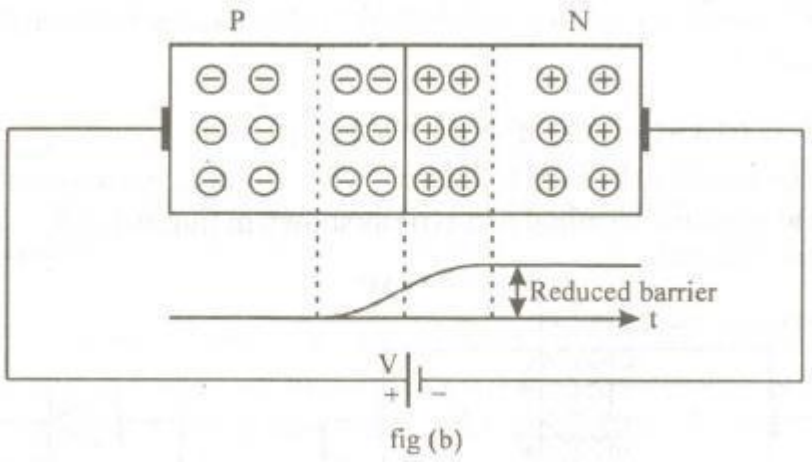


Fig : Reverse biasing of p-n junction

- When the external voltage applied to the junction is in such a direction, that the potential barrier is increased, then it is called reverse biasing.

- To apply reverse bias, connect –ve terminal of the battery to p-type and +ve terminal to n-type as shown in figure .

- The applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore the resultant field at the junction is strengthened and the barrier height is increased as shown in fig

- The increased potential barrier prevents the flow of charge carriers across the junction. Thus a high resistance path is established for the entire circuit and hence current does not flow.

(i) Circuit diagram

(ii) Characteristics

- The V-I characteristics of a semiconductor diode can be obtained with the help of the circuit shown in fig.

- The supply voltage V is a regulated power supply, the diode is forward biased in the circuit shown. The resistor R is a current limiting resistor. The voltage across the diode is measured with the help of voltmeter and the current is recorded using an ammeter.

By varying the supply voltage different sets of voltage and currents are obtained. By plotting these values on a graph, the forward characteristics can be obtained.

- It can be noted from the graph the current remains zero till the diode voltage attains the barrier potential.

- For silicon diode, the barrier potential is 0.7 V and for Germanium diode, it is 0.3 V. The barrier potential is also called as knee voltage or cur-in voltage.

- The reverse characteristics can be obtained by reverse biasing the diode. It can be noted that at a particular reverse voltage, the reverse current increases rapidly. This voltage is called breakdown voltage.

Therefore the value of forward drop of the voltage for *silicon diode is typically 0.7V and that for silicon is 0.3V*.Because the diode reverse current (I_R) is very much smaller than the forward current hence the reverse characteristics are plotted with expanded current scales. For a Si diode I_R is normally less than 100na. and it is almost independent of the reverse bias voltage.Ir is largely a minority charge carrier reverse saturation current. The increase in I due to increase in reverse voltage is very small and is largely due to some minority carriers leaking along the junction surface. For a diode the reverse current is typically less than 1/10,000 of the lowest normal forward current. This quite negligible and may treated as negligible and hence the diode is regarded as open circuit in this condition and hence is an open switch. When the reverse bias on the diode is increased then the device enters into **reverse breakdown.** This can destroy the diode unless limited by an external resistance connected in series. This phenomenon is best made use of in *Zener* diodes discussed later.

Diode current equation

The current in a diode is given by the diode current equation

$I = I_0(e V/\eta VT –1)$

Where, I------ diode current

I_0------ reverse saturation current

V------ diode voltage

η------- semiconductor constan=1 for Ge, 2 for Si.

V_T------ Voltage equivalent of temperature= T/11,600 (Temperature T is in Kelvin)

Note:- If the temperature is given in ^{0}C then it can be converted to Kelvin by the help of following relation, $^0C+273 = K$

Comparision of Si and Ge diodes: The characteristic of the Si diode is similar to those of Ge diode, with some differences as depicted in the figure below.

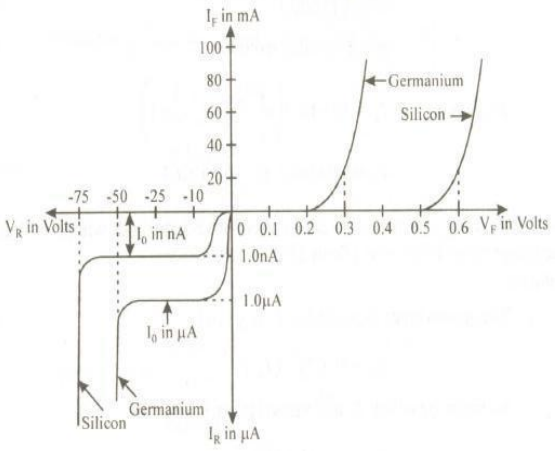


Fig : Comparison of characteristics of Silicon and Germanium diodes

The forward voltage drop of a Ge diode is typically 0.3V, compared to 0.7V for Si. For a Ge device the reverse saturation current at 25^0 C may be around 1μA which is much larger than the reverse saturation current for a Si diode which is around 50 nA. The temperature dependence of the I_R for Ge is more as compared to Si diode.

Finally the reveres breakdown voltage for Ge is lower than that for Si devices.
The lower forward voltage drop for Ge diodes compared to Si diodes can be a distinct advantage.

However ,the lower reverse current and higher reverse breakdown voltage of Si diodes make them preferable to Germanium devices for most applications.

Diode Parameters

Static Resistance and is represented by R_F. It is a constant resistance of the diode at a particular constant forward current. On the contrary the dynamic resistance is change in levels of current

and voltage.

Static Resistance : The static resistance of a diode is the resistance offered by a forward biased diode at a particular point on its V-I characteristics.

Dynamic resistance of the diode is the resistance offered to changing levels of forward current. The dynamic resistance is also known as the **incremental resistance** or **ac resistance** and is the reciprocal of the slope of the forward characteristics beyond the knee as shown in the figure.

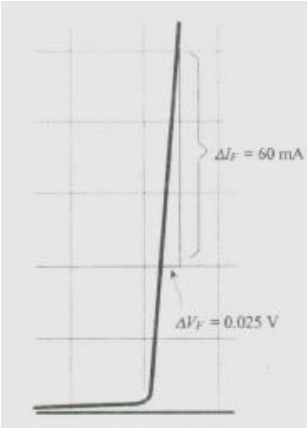


Fig1.11:Determination of diode dynamic resistance from the forward characteristics

Referring to the figure,

$$r_d = \frac{\Delta V_F}{\Delta I_F}$$

Where r_d is the dynamic resistance

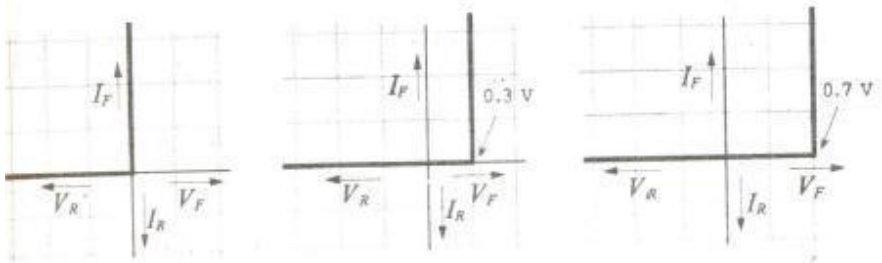
The dynamic resistance can also be calculated from the equation

$$r'_d = \frac{26\ \text{mV}}{I_F}$$

DIODE APPROXIMATIONS

Ideal diode characteristics

We know that a diode is one way device, offering low resistance when forward biased and a high resistance when reverse biased. On the other hand an ***ideal diode*** (a perfect diode) would, zero forward drop and *infinite reverse resistance* and thus behave electrically open circuit. Figure below shows the characteristics of ideal diode.



(a) Ideal diode characteristics (b) Approximate characteristics for a germanium diode (c) Approximate characteristics for a silicon diode

Fig1.12 : ideal diode characteristics

Although an ideal diode does not exist, some situations demand such assumptions where diodes can be assumed to be near ideal devices. In situations, for example, when supply voltages much larger than the diode forward drop V_F is used then the diode forward can be ignored without introducing any serious error.

Also, the diode reverse current is normally so much smaller than the forward current that the reverse current can be ignored. These assumptions lead to the near-ideal, or approximate characteristics for Si and Ge diodes as shown in figure 6(b) and 6(c) below.

Example 1: A silicon diode is used in the circuit shown in Fig. Calculate the diode current.

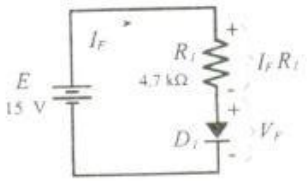


Fig. : Figure for example 1

Solution

$$E = I_F R_1 + V_F$$

or,
$$I_F = \frac{E - V_F}{R_1} = \frac{15\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega}$$

$$= 3.04\text{ mA}$$

Piecewise Linear Characteristic

When the forward characteristic of a diode is not available. A traight-line approximation, called the *piecewise linear characteristic*, may be employed. To construct the piecewise linear characteristic, V_F is first. marked on the horizontal axis, as shown in Fig. 13. Then, starting at V_F,

a straight line is drawn with a slope equal to the diode dynamic resistance. Ex.2 demonstrates the process.

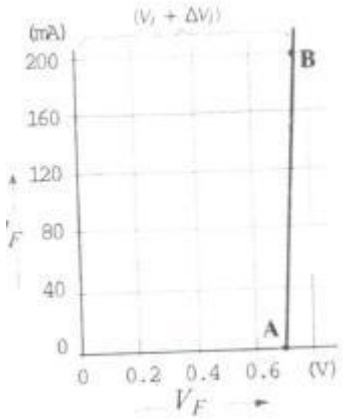


Fig.1.14 : Piecewise Linear Characteristic of a diode

Example 2: Construct the piecewise-linear characteristic for a silicon diode that has a 0.25Ω Dynamic resistance and a 200 mA maximum forward current.

Solution

Plot point A on the horizontal axis at:

$$V_F = 0.7\ V$$

$$\Delta V_F = \Delta I_F \times r_d = 200\ mA \times 0.25\ \Omega$$
$$= 0.05\ V$$

Plot point B (on Fig. 13)at: IF = 200 mAand VF = (0.7V+ 0.05V) Draw the characteristic through points A and B.

Diode equivalent circuit

The equivalent circuit for a device is a circuit representing its internal behavior.

In case of a diode the circuit is made up of a number of components, such as resistors and voltage cells.

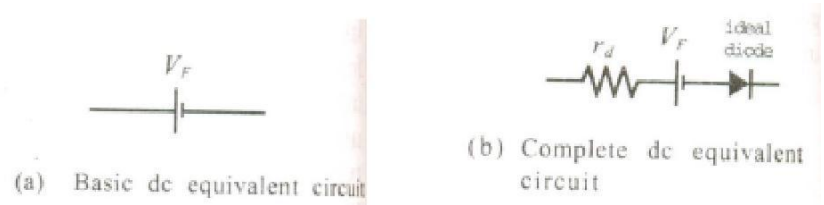


Figure 1.15 : Diode equivalent circuit

An accurate equivalent circuit for the diode includes the dynamic resistance (rd) in series with diode forward drop V_F as shown in the fig. above. This takes into account of the small variations in V_F that occur with change in forward current. With rd included the equivalent circuit represents a diode with the type of piecewise characteristics. Consequently, the circuit is known as piecewise linear equivalent circuit. This equivalent circuit when used in traditional circuit analysis gives accurate results.

AC equivalent circuit of a diode

The ac equivalent circuit is the modification of the dc equivalent circuit discussed earlier and is shown in the figure 18a,b,c, below.

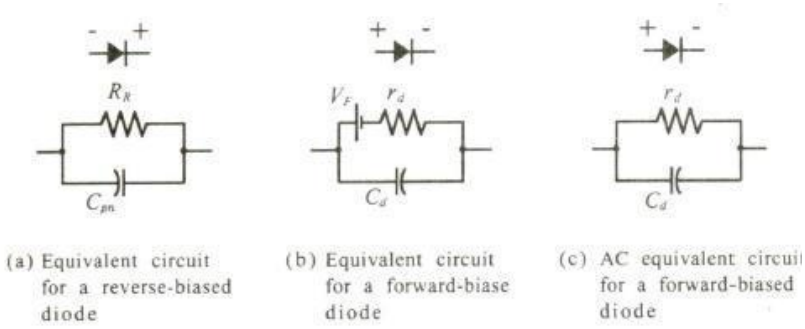


Fig 1.20:Diode capacitance equivalent circuits

When the pn-junction is reverse biased, the equivalent circuit consists of a voltage cell representing cut-in voltage in series with dynamic resistance rd. The whole circuit is a combination of the above parameters connected in parallel with diffusion capacitance and is shown in figure below. Similarly the equivalent circuit of a pn-junction under reverse bias is represented by the reverse bias resistance Rr in parallel combination with depletion capacitances shown in figure.

Breakdown mechanism in diode :

Generally there are two types of mechanisms which give rise to the breakdown of a pn-junction when operated under reverse bias. One is called the ***avalanche breakdown*** and the other is called ***zener breakdown***

Avalanche breakdown

Consider a situation in which a thermally generated carrier (part of reverse saturation current) falls down the junction barrier and acquires energy from the applied potential. This carrier collides with the crystal ion and imparts sufficient energy to disrupt a covalent bond. In addition to the original carrier, a new electron-hole pair has now been generated. These carriers may also pick up sufficient energy from the applied field, collide with another crystal

ion, and create still another electron-hole pair. Thus each new carrier may, in turn, produce additional carriers through collision and the action of disrupting the bonds. This cumulative process is referred to as ***avalanche multiplication*** It results in large reverse currents, and the diode is said to be in the region of ***avalanche breakdown.*** A lightly doped pn junction has a tendency to widen the depletion region under reverse bias, and enter into avalanche breakdown.

Zener breakdown

In this kind of breakdown it is possible to initiate breakdown through a direct rupture of the bonds. The field intensity increases as the impurity concentration increases, for a fixed applied voltage Because of the existence of the electric field at the junction, sufficiently strong force may be exerted on a bound electron by the field to tear it out of its covalent bond. The new hole electron pair which is created increases the reverse current. This process is called ***Zener breakdown***. Note this process does not involve collision of carriers with the crystal ions as does in avalanche multiplication.

Zener diode is heavily doped and is designed to operate under reverse bias condition. Under this condition it found that the zener breakdown occurs at a field of approximately $2*10^7$V/m.This value is reached at voltages below about 6V for heavily doped diodes.

For lightly doped diodes the breakdown voltage is higher, and avalanche multiplication is the predominant effect.

Due to heavy doping of p and n regions, the depletion width is very small and for an applied reverse bias of 6V or less, the electric field across the depletion region becomes very high in the order of $2*10^7$V/m,resulting breakdown is in the range of 5 to 8V

Key point :***For a zener diode the p and n layers of the diode is heavily doped and hence the mechanism of breakdown is zener breakdown.***

For a regular diode the p and n layers of the diode is lightly doped and hence the mechanism

of breakdown is avalanche breakdown.

Zener diode

The zener diode is a pn-junction silicon diode which is heavily doped and designed to operate under reverse bias condition, these diodes for their operation depends on the reverse breakdown. When once the diode breaks down the voltage across the diode remains constant, converting the excess voltage into current and thus maintaining the voltage across it constant, hence these diodes are very useful as voltage reference or constant voltage devices.

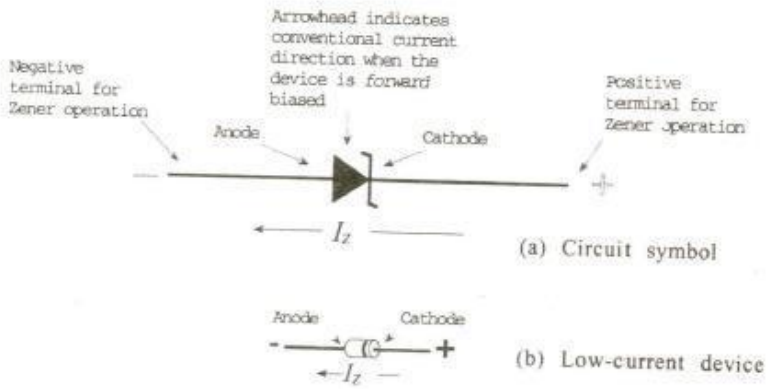


Fig 1.22 :Zener diode symbol

Diodes designed to operate under reverse breakdown are found to be extremely stable over wide range of current levels, but maintaining voltage across the device constant. The popular voltage range for use in electronic circuits is from 2.4V to 15V, with currents less than 100mA.The desired amount of zener breakdown V_Z can be achieved by controlling the doping during the manufacture of diodes.

The zener diode when operated under forward bias has the characteristics similar to ordinary diodes. In the zener diode symbol the direction of the arrow continues to indicate the conventional current direction under forward bias condition

2.9 Zener Diode characteristics

The reverse voltage characteristics of a semiconductor diode including the breakdown region is shown below.

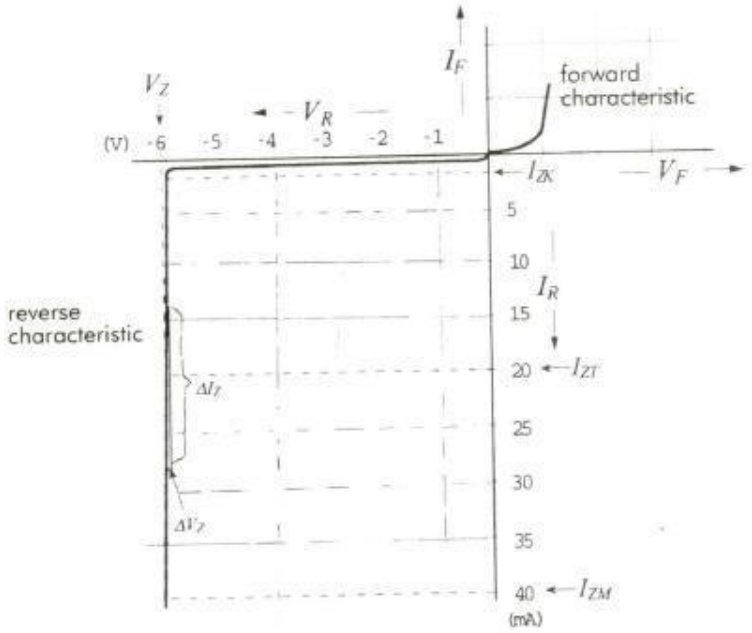


Fig.1.23: Zener diode characteristics

Zener diodes are the diodes which are designed to operate in the breakdown region. They are also called as Breakdown diode or Avalanche diodes.

Half wave diode rectifiers

RECTIFIERS

"Rectifiers are the circuit which converts ac to dc"

Rectifiers are grouped into two categories depending on the period of conductions.

1. **Half-wave rectifier**
2. **Full- wave rectifier.**

Half-wave rectifier

The circuit diagram of a half-wave rectifier is shown in fig. 22 below along with the I/P and O/P waveforms.

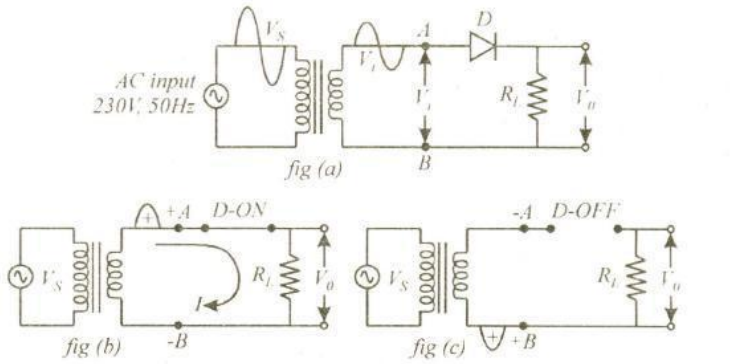


Fig. 1.24 Half wave rectifier, fig-a half wave rectifier circuit, fig-b when diode is conducting and, fig-c, when diode is not conducting.

- The transformer is employed in order to step-down the supply voltage and also to prevent from shocks.
- The diode is used to rectify the a.c. signal while , the pulsating d.c. is taken across the load resistor R_L.
- During the +ve half cycle, the end X of the secondary is +ve and end Y is -ve . Thus , forward biasing the diode. As the diode is forward biased, the current flows through the load R_L and a voltage is developed across it.
- During the –ve half-cycle the end Y is +ve and end X is –ve thus, reverse biasing the diode. As the diode is reverse biased there is no flow of current through R_L thereby the output voltage is zero.

The waveforms of a half wave rectifier is shown in figure 1.25 when diode is conducting and diode is not conducting.

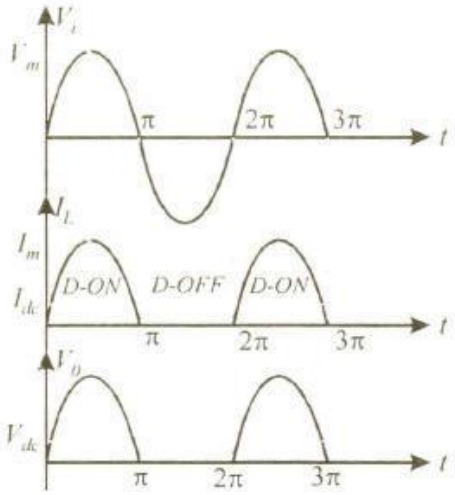


Fig. : Waveforms of a half wave rectifier

From the circuit it is clear that

$$V_0 = V_m \sin \omega t \quad for \ 0 \le \omega t \le \pi$$

$$V_0 = 0 \quad for \ \pi \le \omega t \le 2\pi$$

V_i is a sinusoidal waveform it can be represented mathematically as

$$V_i = V_m \sin \omega t = V_m \sin \theta$$

During positive half cycle from 0 *to* π.

$$i = I_m \sin \theta \ for \ 0 \le \theta \le \pi$$

Similarly during negative half cycle from π *to* 2π

$$i = 0 \ for \ \pi \le \theta \le 2\pi$$

The maximum load current is given by

$$I_m = \frac{V_m}{R_f + R_S + R_L}$$

Where R_f is forward resistance of diode, $R_f = 0$ (ideal).

R_S is transformer secondary winding resistance, R_L is load resistance.

DC OR AVERAGE CURRENT I_{DC}

$$\text{Average value} = \frac{\text{Area under the curve over the full}}{\text{Time period}}$$

$$I_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\theta d\theta + \int_{\pi}^{2\pi} 0 d\theta\right]$$

$$I_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\theta d\theta\right]$$

$$I_{dc} = \frac{I_m}{2\pi}[-\cos\theta]_0^{\pi}$$

$$I_{dc} = \frac{-I_m}{2\pi}[\cos\pi - \cos 0]$$

$$I_{dc} = \frac{-I_m}{2\pi}[-1-1]$$

$$I_{dc} = \frac{-I_m}{2\pi}[-2]$$

$$I_{dc} = \frac{I_m}{\pi} \quad or \quad I_{dc} = 0.318 I_m$$

Since $I_m = \dfrac{V_m}{R_f + R_S + R_L}$

$$V_{dc} = I_{dc} R_L$$

$$V_{dc} = \frac{I_m R_L}{\pi}$$

Substitute I_m in equation-2.5 we get

$$V_{dc} = \frac{V_m R_L}{\pi\left(R_f + R_L + R_S\right)}$$

$$V_{dc} = \frac{V_m}{\pi\left(\dfrac{R_f + R_S}{R_L} + 1\right)}$$

If R_f & R_S are neglected compared to R_L then

$$V_{dc} = \frac{V_m}{\pi} \quad or \quad V_{dc} = 0.318 V_m$$

ROOT MEAN SQUARE LOAD CURRENT (I_{RMS})

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d\theta}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\theta d\theta}\,; \qquad \text{since } i = 0 \text{ for } \pi \text{ to } 2\pi$$

$$I_{rms} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}(1-\cos 2\theta) d\theta}$$

$$I_{rms} = 0.5 I_m = \frac{0.5 V_m}{R_L}$$

RMS value of load voltage

$$V_{rms} = I_{rms} R_L$$

$$V_{rms} = \frac{I_m}{2} R_L ; \quad \text{Since } I_{rms} = \frac{I_m}{2}$$

$$V_{rms} = \frac{V_m R_L}{2\left(R_f + R_S + R_L\right)} ; \quad \text{Since } I_m = \frac{V_m}{R_f + R_L + R_S}$$

If $R_f + R_S < R_L$ then

$$V_{rms} \approx \frac{V_m}{2}$$

The output of half wave rectifier is unidirectional, but in practice it is pulsating DC rather than a steady DC, the output of rectifier contains DC and AC components, the undesired AC components across rectifier output is called as ripples.

How effectively a HWR converts AC power to DC power is described quantitatively by a term called ripple factor.

$$r = \frac{\text{rms value of AC component of output voltage}}{\text{DC component of output voltage}} = \frac{I_{ac}}{I_{dc}}$$

We get, rms value of the ac component of current is given by $I_{rms}^2 = I_{dc}^2 + I_{ac}^2$

$$I_{ac}^2 = I_{rms}^2 - I_{dc}^2$$

$$r = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

$$r = \sqrt{\frac{\pi^2}{4} - 1}$$

$$r = \sqrt{(1.57)^2 - 1} = 1.21$$

$r = 1.21$ in terms of percentage $r = 121\%$

EFFICIENCY OF RECTIFICATION (η)

The efficiency of rectification is the ratio of the output power to the input power, but in

rectifiers it is defined as ratio of output DC power to the input AC power.

The PIV rating of the diode is given by manufacturer and the diode should be operated below its PIV.If the max. voltage across the secondary of the transformer exceeds PIV of the diode then the diode will get damaged.

For HWR the PIV under reverse bias condition is V_m.

Advantage and disadvantages of HWR.

Advantage: 1.The circuit is simpler and requires only one diode.
2. PIV of the diode is only V_m.

Disadvantages: 1. The ripple is more and hence the ripple factor is also more(12%) 2 Efficiency is very low.(40.6%)

Low TUF (28.7%

Full-wave rectifier

Full-wave rectifier is of two types

1. Centre tapped full-wave rectifier
2. Bridge rectifier

Centre tapped full –wave rectifier

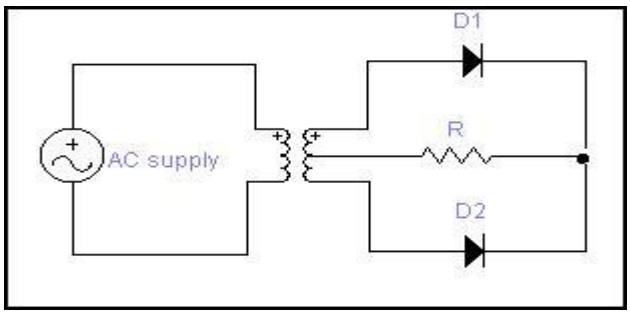


Fig. 1.26 Centre tapped full-wave rectifier

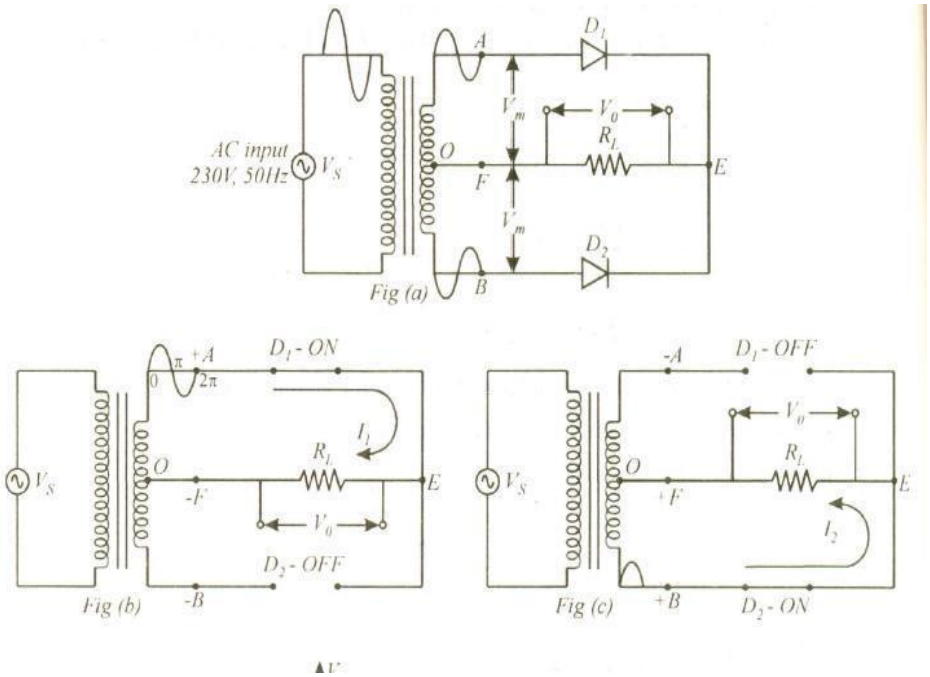


Fig. 1.27 Full wave rectifier, fig-a full wave rectifier circuit, fig-b when diodes are conducting and, fig-c, when diode s are not conducting.

- The circuit diagram of a center tapped full wave rectifier is shown in fig. 1.26 above. It employs two diodes and a center tap transformer. The a.c. signal to be rectified is applied to the primary of the transformer and the d.c. output is taken across the load $R_{L.}$

- During the +ve half-cycle end X is +ve and end Y is –ve this makes diode D_1 forward biased and thus a current i_1 flows through it and load resistor R_L.Diode D_2 is reverse biased and the current i_2 is zero.
- During the –ve half-cycle end Y is +Ve and end X is –Ve. Now diode D_2 is forward biased and thus a current i_2 flows through it and load resistor R_L. Diode D_1 is reversed and the current i_1 =.

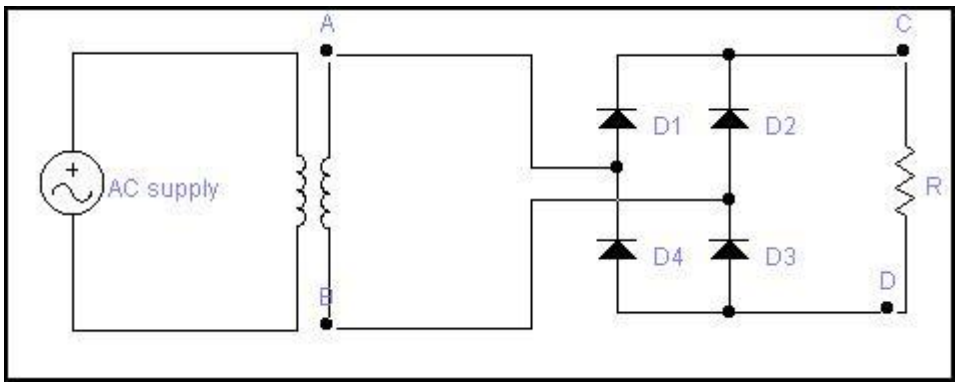
Advantages

- Efficiency is high, (81.2%).
- Low ripple, ripple factor is 48.2%.
- Requires only two diodes.

Disadvantages

- Since, each diode uses only one-half of the transformer secondary voltage the d.c. output is comparatively small.
- The diodes used must have high Peak-inverse voltage, PIV=$2V_m$.
- Requirement of a special-centre tapped- transformer

Bridge rectifier



(i)

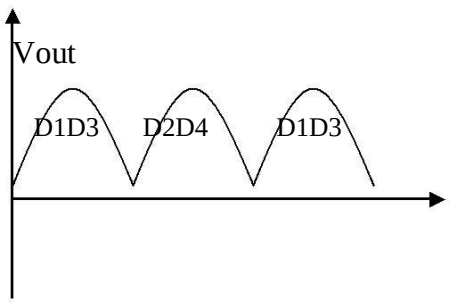


Fig.1.28 Full wave bridge wave rectifier (i) Circuit diagram (ii) waveforms.

- The circuit diagram of a bridge rectifer is shown above. It uses four diodes and a transformer.

- During the +ve half-cycle, end A is +ve and end B is –ve thus diodes D_1 and D_3 are forward bias while diodes D_2 and D_4 are reverse biased thus a current flows through diode D_1, load R_L (C to D) and diode D_3.

- During the –ve half-cycle, end B is +ve and end A is –ve thus diodes D_2 and D_4 are forward biased while the diodes D_1 and D_3 are reverse biased. Now the flow of current is through diode D_4 load R_L (D to C) and diode D_2. Thus, the waveform is same as in the case of center-tapped full wave rectifier.

Advantages

- The need for center-taped transformer is eliminated.
- The output is twice when compared to center-tapped full wave rectifier. for the same secondary voltage.
- The peak inverse voltage is one-half(1/2) compared to center-tapped full wave rectifier.
- Can be used where large amount of power is required.

Disadvantages

- It requires four diodes.
- The use of two extra diodes cause an additional voltage drop thereby reducing the output voltage.
-

Analysis of Full Wave Rectifier (FWR)

The analysis of FWR's –center tap construction or bridge construction- is same except for minor changes.

The full wave rectifier (FWR), will have 48.2% ripple. Comparing this with that of HWR which is 121%, we find that the ripple factor is better for FWR.

Efficiency of Full-wave rectifier

Let $V = V_m \sin\theta$ be the voltage across the secondary winding I

$= I_m \sin\theta$ be the current flowing in secondary circuit

r_f = diode resistance

R_L = load resistance

dc power output

$$P_{dc} = I_{dc}^2 R_L \quad \text{----------(1)}$$

$$I_{dc} = I_{av} = 2\frac{1}{2\pi}\int_0^{\pi}$$

$$I_{av} = 2\frac{1}{2\pi}\int_0^{\pi} \text{Im}\theta \; .d\theta$$

$$I_{av} = \frac{2I_m}{\pi} \qquad (2)$$

Efficiency of Full-wave rectifier

Let V = $V_m \sin\theta$ be the voltage across the secondary winding I
= $I_m \sin\theta$ be the current flowing in secondary circuit
r_f = diode resistance
R_L = load resistance

Efficiency=dc power output/acpower input=Pdc/Pac
dc power output

$$Pdc = I_{dc}^2 R_L \text{ ----------} \qquad (1)$$

$$I_{dc} = I_{av} = 2\frac{1}{2\pi}\int_0^{\pi} i.d\theta$$

$$I_{av} = 2\frac{1}{2\pi}\int_0^{\pi} \text{Im}\, Sin\theta.d\theta$$

$$I_{av} = \frac{2I_m}{\pi} \qquad (2)$$

$$\therefore P_{dc} = \left(\frac{2I_m}{\pi}\right)^2 R_L \qquad (3)$$

input ac power

$$P_{ac} = I_{rms}^2 \left(r_f + R_L\right) \text{ ----------} \qquad (4)$$

$$I_{rms} = \sqrt{2\frac{1}{2\pi}\int_0^{\pi} i^2 d\theta}$$

Squaring both sides we get

$$I_{rms}^2 = \frac{1}{\pi}\int_0^{\pi} i^2 d\theta$$

$$I_{rms}^2 = \frac{1}{\pi}\int_0^{\pi} (\text{Im}\, Sin\theta)^2 d\theta$$

$$I_{rms}^2 = \frac{I_m^2}{2}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \qquad (5)$$

$$\therefore P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 \left(r_f + R_L\right) \qquad (6)$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} * \frac{R_L}{\left(r_f + R_L\right)}$$

$$\eta = \frac{0.812}{1 + \frac{r_f}{R_L}} \qquad (7)$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

Maximum efficiency = 81.2 %

This is the double the efficiency due to half wave rectifier. Therefore a Full-wave rectifier is twice as effective as a half-wave rectifier

Comparision of Rectifiers

Particulars	**Half wave rectifier**	**Centre-tapped Full wave rectifier**	**Bridge rectifier**
1. No. of diodes	1	2	4
2. I_{dc}	I_m / Π	$2I_m /\Pi$	$2I_m /\Pi$
3. V_{dc}	V_m / Π	$2V_m / \Pi$	$2V_m / \Pi$
4.I_{rms}	$I_m / 2$	$I_m /\sqrt{2}$	$I_m /\sqrt{2}$
5.Efficiency	40.6 %	81.2 %	81.2 %
6.PIV	V_m	$2V_m$	V_m
7.Ripple factor	1.21	0.48	0.48

Note:

- The relation between turns ratio and voltages of primary and secondary of the transformer is given by
  - $N_1 / N_2 = V_p / V_s$

- RMS value of voltage and Max. value of voltage is related by the equation.
  - $V_{rms} = V_m / \sqrt{2}$ (for full-cycle of ac)

- If the type of diode is not specified then assume the diode to be of silicon type.
- For an ideal diode, forward resistance $r_f = 0$ and cut-in voltage , $V_\gamma = 0$.

The Transformer Utilization Factor (TUF) for full wave rectifier is 81.2%,which is better compared to HWR,for which it is only28.7%.

Peak Inverse Voltage(PIV): For the center tapped transformer if any one diode is conducting the voltage across it is the entire secondary voltage of the transformer which is V_m.+ V_m.=2V_m.Therefore the diodes used in the center tap design should have a PIV of 2V_m.Whereas in the bridge configuration the PIV of each diode is only V_m

Note:

The relation between turns ratio and voltages of primary and secondary of the transformer is given by

$$N_1 / N_2 = V_p / V_s$$

- RMS value of voltage and Max. value of voltage is related by the equation.
  - $V_{rms} = V_m / \sqrt{2}$ (for full-cycle of ac)
- If the type of diode is not specified then assume the diode to be of silicon type.
- For an ideal diode, forward resistance $r_f = 0$ and cut-in voltage , $V_\gamma = 0$.

TRANSISTORS

A transistor is a sandwich of one type of semiconductor (P-type or n-type) between two layers of other types.

Transistors are classified into two types;

1. **pnp transistor**

   pnp transistor is obtained when a n-type layer of silicon is sandwiched between two p-type silicon material.

2. **npn transisitor**

   npn transistor is obtained when a p-type layer of silicon is sandwiched between two n-type silicon materials.

Figure2.1 below shows the schematic representations of a transistor which is equivalent of two diodes connected back to back.

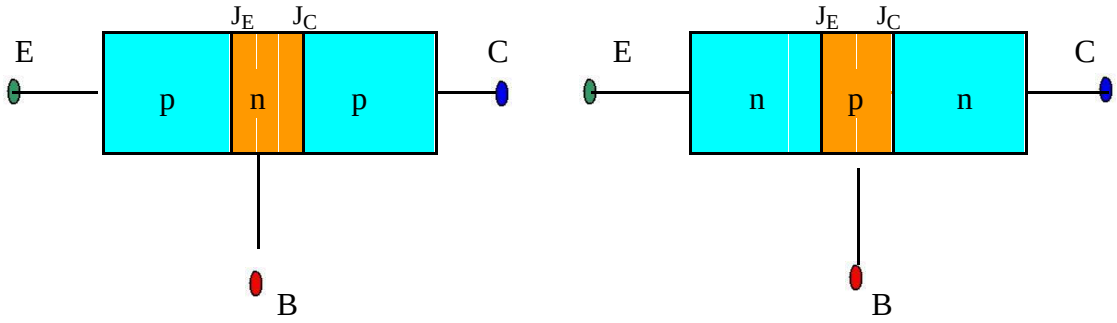


Fig 2.1: Symbolic representation

Fig 2.2: Schematic representation

- The three portions of transistors are named as emitter, base and collector. The junction between emitter and base is called emitter-base junction while the junction between the collector and base is called collector-base junction.
- The base is thin and tightly doped, the emitter is heavily doped and it is wider when compared to base, the width of the collector is more when compared to both base and emitter.
- In order to distinguish the emitter and collector an arrow is included in the emitter. The direction of the arrow depends on the conventional flow of current when emitter base junction is forward biased.
- In a pnp transistor when the emitter junction is forward biased the flow of current is from emitter to base hence, the arrow in the emitter of pnp points towards the base.

Operating regions of a transistor

A transistor can be operated in three different regions as

a) active region
b) saturation region
c) cut-off region

Active region

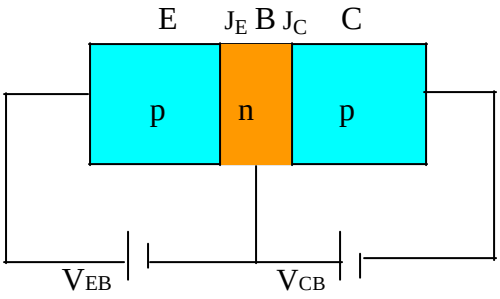


Fig 2.3: pnp transistor operated in active region

The transistor is said to be operated in active region when the emitter-base junction is forward biased and collector –base junction is reverse biased. The collector current is said to have two current components one is due to the forward biasing of EB junction and the other is due to reverse biasing of CB junction. The collector current component due to the reverse biasing of the collector junction is called reverse saturation current (I_{CO} or I_{CBO}) and it is very small in magnitude.

Saturation region

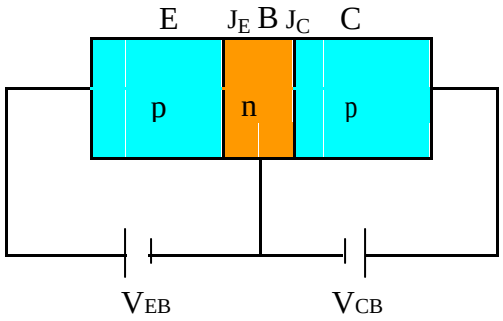


Fig: pnp transistor operated in Saturation region

Transistor is said to be operated in saturation region when both EB junction and CB junction are forward biased as shown. When transistor is operated in saturation region I_C increases rapidly for a very small change in V_C.

Cut-off region

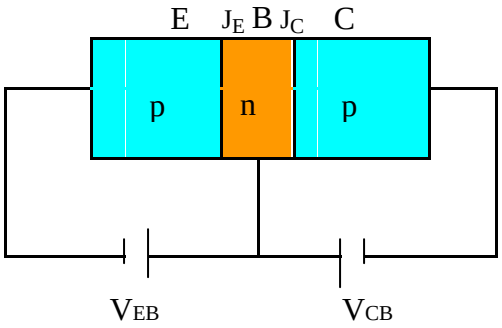


Fig : pnp transistor operated in Cut-off region

When both EB junction and CB junction are reverse biased, the transistor is said to be operated in cut-off region. In this region, the current in the transistor is very small and thus when a transistor in this region it is assumed to be in off state.

Working of a transistor (pnp)

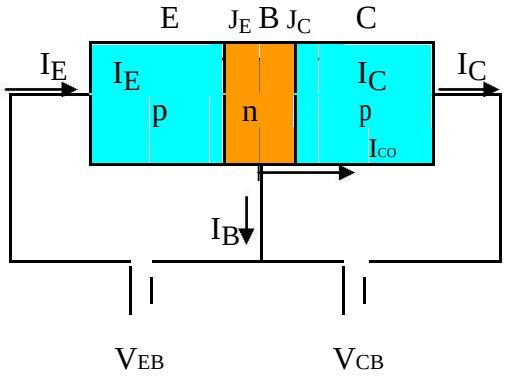


Fig 2.6 Transistor in active region

- Consider a pnp transistor operated in active region as shown in Figure 2.6

- Since the EB junction is forward biased large number of holes present in the emitter as majority carriers are repelled by the +ve potential of the supply voltage V_{EB} and they move towards the base region causing emitter current I_E.

- Since the base is thin and lightly doped very few of the holes coming from the emitter recombine with the electrons causing base current I_B and all the remaining holes move towards the collector. Since the CB junction is reverse biased all the holes are immediately attracted by the –ve potential of the supply V_{CB}. Thereby giving rise to collector current I_C.

- Thus we see that $I_E = I_B + I_C$ ----------(1) (By KVL)

- Since the CB junction is reverse biased a small minority carrier current I_{CO} flows from base to collector.

Current components of a transistor

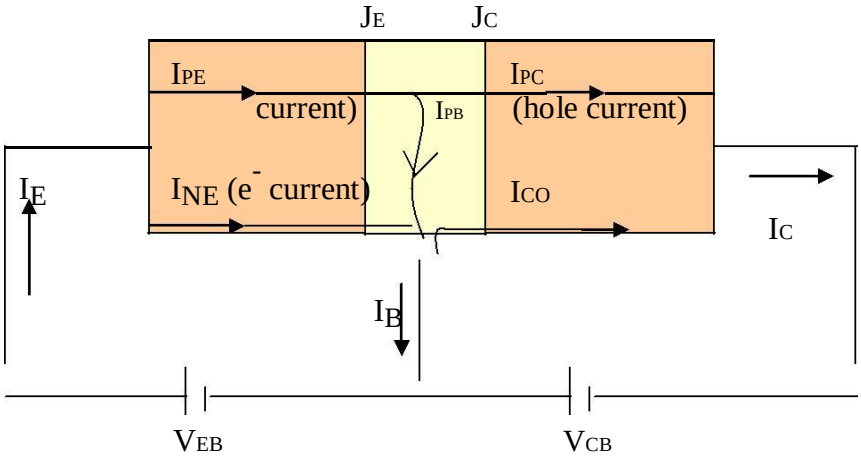


Fig 2.7: Current components of a transistor

Fig 2.7 above shows a transistor operated in active region. It can be noted from the diagram the battery V_{EB} forward biases the EB junction while the battery V_{CB} reverse biases the CB junction.

As the EB junction is forward biased the holes from emitter region flow towards the base causing a hole current I_{PE}. At the same time, the electrons from base region flow towards the emitter causing an electron current I_{NE}. Sum of these two currents constitute an emitter current $I_E = I_{PE} + I_{NE}$.

The ratio of hole current I_{PE} to electron current I_{NE} is directly proportional to the ratio of the conductivity of the p-type material to that of n-type material. Since, emitter is highly doped when compared to base; the emitter current consists almost entirely of holes.

Not all the holes, crossing EB junction reach the CB junction because some of the them combine with the electrons in the n-type base. If I_{PC} is the hole current at (Jc) CB junction. There will be a recombination current $I_{PE} - I_{PC}$ leaving the base as shown in figure 3.7.

If emitter is open circuited, no charge carriers are injected from emitter into the base and hence emitter current I_E =o. Under this condition CB junction acts a a reverse biased diode and therefore the collector current ($I_C = I_{CO}$) will be equal to te reverse saturation current. Therefore when EB

junction is forward biased and collector base junction is reverse biased the total collector current $I_C = I_{PC} + I_{CO}$.

Transistor configuration

We know that, transistor can be used as an amplifier. For an amplifier, two terminals are required to supply the weak signal and two terminals to collect the amplified signal. Thus four terminals are required but a transistor is said to have only three terminals Therefore, one terminal is used common for both input and output.

This gives rise to three different combinations.

1. Common base configuration (CB)
2. Common emitter configuration (CE)

1. CB configuration

A simple circuit arrangement of CB configuration for pnp transistor is shown below.

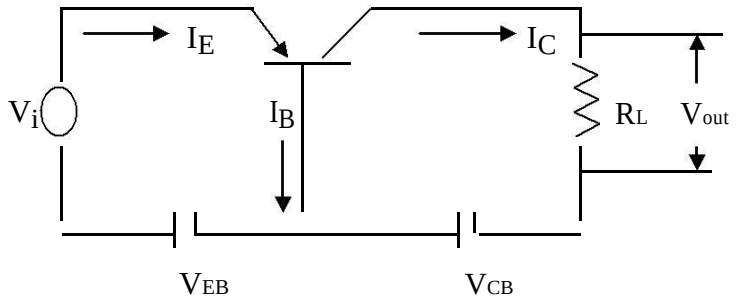


Fig 2.8:CB configuration

In this configuration, base is used as common to both input and output. It can be noted that the i/p section has an a.c. source V_i along with the d.c. source V_{EB}. The purpose of including V_{EB} is to keep EB junction always forward biased (because if there is no V_{EB} then the EB junction is forward biased only during the +ve half-cycle of the i/p and reverse biased during the –ve half cycle). In CB configuration, I_E –i/p current, I_C –o/p current.

Current relations

1.current amplification factor (α)

It is defined as the ratio of d.c. collector current to d.c. emitter current

$$\alpha = \frac{I_o}{I_E}$$

2. Total o/p current

We know that CB junction is reverse biased and because of minority charge carriers a small reverse saturation current I_{CO} flows from base to collector.

$I_C = I_E + I_{CO}$

Since a portion of emitter current I_E flows through the base ,let remaining emitter current be αI_E .

$\mathbf{I_C = \alpha I_E + I_{C}o}$

Characteristics

1. **Input characteristics**

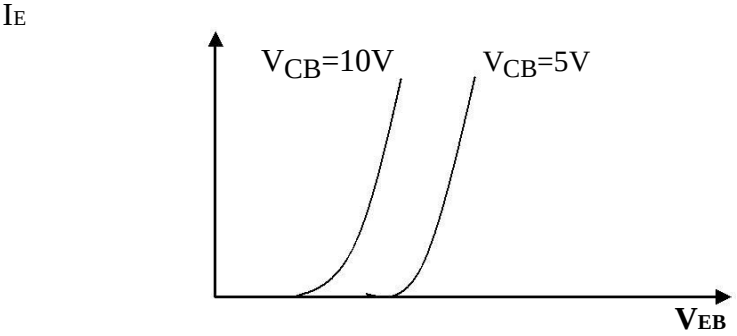


Fig 2.9: Input characteristics

I/p characteristics is a curve between I_E and emitter base voltage V_{EB} keeping V_{CB} constant. I_E is taken along y-axis and V_{EB} is taken along x-axis. From the graph following points can be noted.

1. For small changes of V_{EB} there will be a large change in I_E. Therefore input resistance is very small.
2. I_E is almost independent of V_{CB}
3. I/P resistance , $R_i = V_{EB} / I_E$ $\downarrow V_{CB}$ =constant

2. Output characteristics

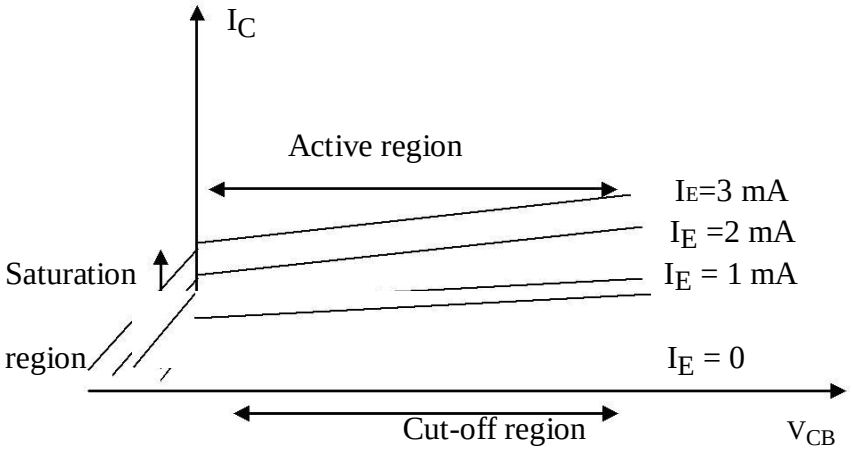


Fig 2.10:Output characteristics

o/p characteristics is the curve between I_C and V_{CB} at constant I_E. The collector current I_C is taken along y-axis and V_{CB} is taken along x-axis. It is clear from the graph that the o/p current I_C remains almost constant even when the voltage V_{CB} is increased.

i.e. , a very large change in V_{CB} produces a small change in I_C. Therefore, output resistance is very high.

O/p resistance $R_o = \Delta V_{EB} / I_C$ I_E = constant

Region below the curve $I_E = 0$ is known as cut-off region where I_C is nearly zero. The region to the left of $V_{CB} = 0$ is known as saturation region and to the right of $V_{CB} = 0$ is known as active region.

2. CE configuration

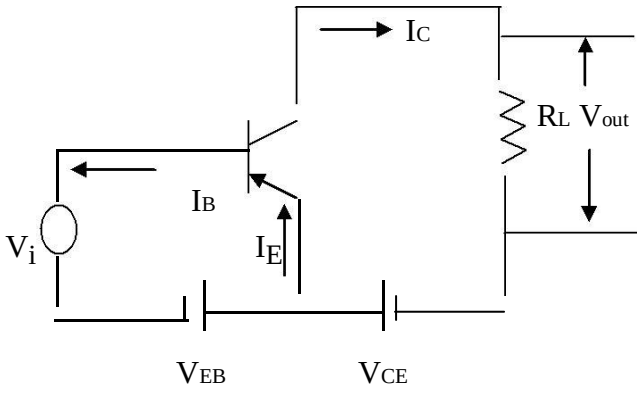


Fig :CE configuration

In this configuration the input is connected between the base and emitter while the output is taken between collector and emitter. For this configuration I_B is input current and I_C is the output current.

1. Current amplification factor (β)

It is the ratio of d.c. collector current to d.c. base current. i.e., $\boldsymbol{\beta = I_C / I_B}$

2. Relationship between α and β

We know that $\alpha = \frac{I_C}{I_E}$

$$\alpha = \frac{I_C}{I_B + I_C}$$

divide both numerator and denominator of RHS by I_C, we get

$$\alpha = \frac{1}{\frac{I_B}{I_C} + 1}$$

Transistor Characteristics

1. i/p characteristics

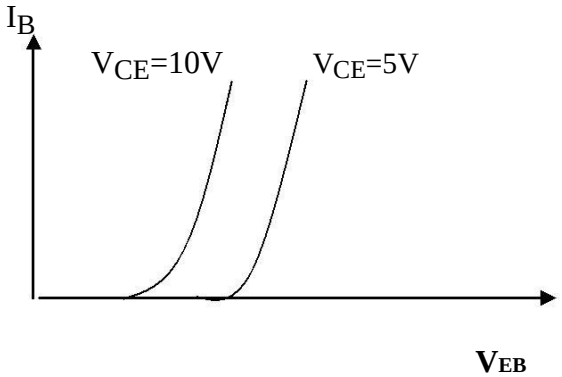


Fig 2.11: i/p characteristics

Input characteristics is a curve between EB voltage (V_{EB}) and base current (I_B) at constant V_{CE}. From the graph following can be noted.

1. The input characteristic resembles the forward characteristics of a p-n junction diode.
2. For small changes of V_{EB} there will be a large change in base current I_B. i.e., input resistance is very small.
3. The base current is almost independent of V_{CE}.
4. Input resistance , $R_i = V_{EB} / I_B \; V_{CE}$ = constant

2. Output characteristics

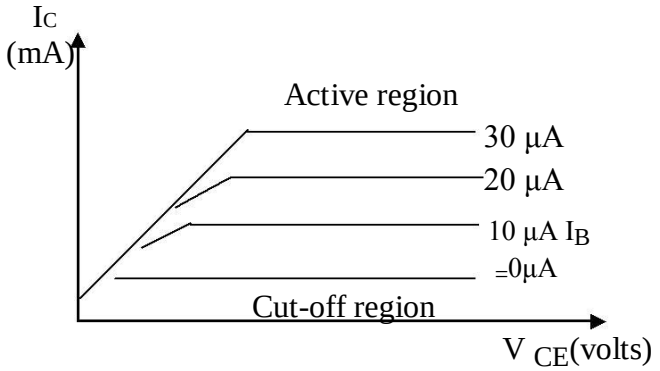


Fig 2.12: Output characteristics

It is the curve between V_{CE} and I_C at constant I_B. From the graph we can see that,

1. Very large changes of V_{CE} produces a small change in I_C i.e output resistance is very high.
2. output resistance $R_o = \Delta V_{CE} / \Delta I_C \; | I_B$ = constant

Region between the curve I_B =0 is called cut-off region where I_B is nearly zero. Similarly the active region and saturation region is shown on the graph.

2. Relationship between α β and γ

$$\gamma = \frac{I_E}{I_B}$$

$$\gamma = \frac{I_B + I_C}{I_B}$$

divide both Numerator and denominator by I_B

$$\gamma = \frac{1 + I_C / I_B}{1}$$

$$\gamma = 1 + \beta \qquad (\beta = I_C / I_B)$$

$$\gamma = 1 + \frac{\alpha}{1 - \alpha}$$

$$\gamma = \frac{1}{1 - \alpha}$$

Derivation of total output current I_E

We know that $I_C = \alpha I_E + I_{CBO}$

$$I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$I_E = \gamma I_B + \gamma I_{CBO}$$

$$\boxed{I_E = \gamma (I_B + I_{CBO})}$$

Comparison between CB, CC and CE configuration

Characteristics	CB	CE	CC
1. Input reistance ($R_{i)}$	low	low	high
2. Output resistance (R_o)	high	high	low
3. Current amplification factor	$\alpha = \frac{\beta}{1+\beta}$	$\beta = \frac{\alpha}{1-\alpha}$	$\gamma = \frac{1}{1-\alpha}$
4. Total output current	$I_C = \alpha I_E + I_{CBO}$	Ic = $\beta I_B + (1+\beta) I_{CBO}$	$I_E = \gamma I_B + \gamma I_{CBO}$
5. Phase relationship between input and output	In-phase	Out-of phase	in-phase
6. Applications	For high frequency applications	For audio frequency applications	For impedance matching
7. Current gain	Less than unity	Greater than unity	Very high
8. Voltage gain	Very high	Grater than unity	Less than unity

Transistor as an amplifier

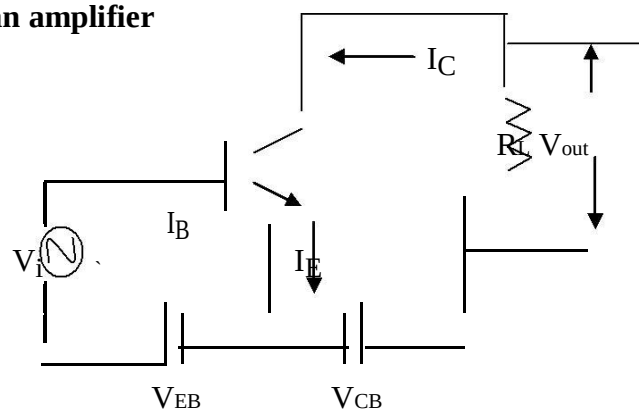


Fig : Transistor as an amplifier

Consider a npn transistor in CE configuration as shown above along with its input characteristics.

A transistor raises the strength of a weak input signal and thus acts as an amplifier. The weak signal to be amplified is applied between emitter and base and the output is taken across the load resistor R_C connected in the collector circuit.

In order to use a transistor as an amplifier it should be operated in active region i.e. emitter junction should be always FB and collector junction should be RB. Therefore in addition to the a.c. input source V_i two d.c. voltages V_{EB} and V_{CE} are applied as shown. This d.c. voltage is called bias voltage.

As the input circuit has low resistance, a small change in te signal voltage V_i causes a large change in the base current thereby causing the same change in collector current (because $I_C = \beta I_B$).

The collector current flowing through a high load resistance R_C produces a large voltage across it. Thus a weak signal applied at the input circuit appears in the amplified form at the output. In this way transistor acts as an amplifier.

Example: Let $R_C = 5K\Omega$, $V_{in} = 1V$, $I_C = 1mA$ then output $V = I_C R_C = 5V$

mass system illustrates some important and universal principles of osc2. CE configuration

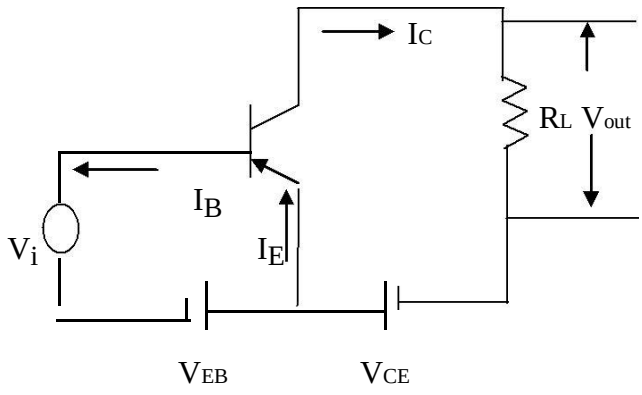


Fig 2.15:CE configuration

In this configuration the input is connected between the base and emitter while the output is taken between collector and emitter. For this configuration I_B is input current and I_C is the output current.

1. Current amplification factor (β)

It is the ratio of d.c. collector current to d.c. base current. i.e., $\boldsymbol{\beta = I_C / I_B}$

2. Relationship between α and β

We know that $\alpha = \frac{I_C}{I_E}$

$$\alpha = \frac{I_C}{I_B + I_C}$$

divide both numerator and denominator of RHS by I_C, we get

$$\alpha = \frac{1}{\frac{I_B}{I_C} + 1}$$

$$\alpha = \frac{1}{\frac{1}{\beta} + 1} \qquad (I_C / I_B = \beta)$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

Also we have

$\alpha(1+\beta) = \beta$

$\alpha + \alpha\beta = \beta$

$\alpha = \beta - \alpha\beta$

$\alpha = \beta(1-\alpha)$

$$\beta = \frac{\alpha}{1-\alpha}$$

Derivation of Total output current I_C

We have $I_C = \alpha I_E + I_{CBO}$

$$I_C = \frac{\beta}{1+B} I_E + I_{CBO}$$

$$\boxed{I_C = \frac{\beta I_E + (1+\beta) I_{CBO}}{1+\beta}}$$

$$Ic = \beta I_B + (1+\beta) I_{CBO}$$

MODULE-2

BIASING METHODS

Biasing:

Transistor biasing is the establishment of suitable dc values such as Ic, V_{CE}, I_B etc. by using a single dc source... When BJT is properly biased, faithful amplification of signals take place. For example applying forward bias to EB- junction and reverse bias to the CB-junction makes the transistor to operate in the active region. Hence ***Biasing is applying dc voltages to the junctions of the transistor to make it operate in the desired region.*** Biasing eliminates the need for separate dc sources in the emitter and collector circuits.

Types of biasing.

There are mainly three types of biasing circuits used for biasing a transistor, they are:

a) Base bias or fixed bias

b) Collector to base bias

c) Voltage divider bias

The three biasing circuits are shown in figure 3.1

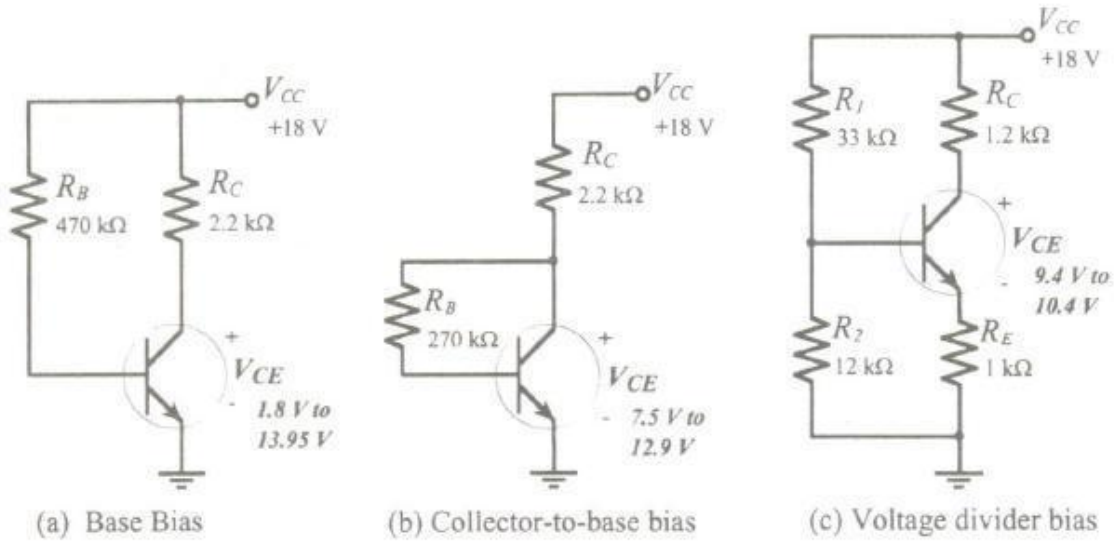


Fig3.1 : The three basic biasing circuits.

a) Base bias or fixed bias:

For this configuration the biasing arrangement is as shown in figure3.2 below. A base resistance R_B is used between Vcc and base to establish the base current I_B Thus the base current is the constant quantity determined by Vcc and I_B. Because Vcc and R_B are fixed quantities, I_B remains fixed and hence it is also called fixed bias.

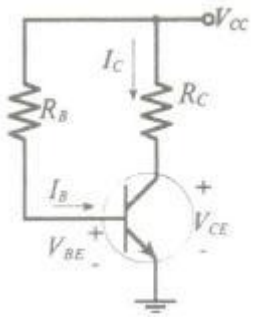


Fig 3.2: Base bias circuit.

Applyingh Kirchoff's voltage law to the base circuirt. (The base circuit consists of Vcc, R_B,EB-junction of the transistor and ground)

$$I_B R_B + V_{BE} = Vcc$$
$$I_B = (Vcc - V_{BE}) / R_B$$

V_{BE} is 0.7V for Silicon and 0.3V for Germanium transistor. The collector current is calculated as

$$Ic = \beta I_B.$$

Applying the KVL to collector circuit (The collector circuit consists of Vcc, Rc, V_{CE}, and ground $Vcc = V_{CE} + IcRc$

$$V_{CE} = Vcc - IcRc$$

Example: The base bias circuit is shown in fig 3.3.For the values indicated calculate I_B, Ic and V_{CE}.

Example1:

The base bias circuit in Fig. 5-13 has $R_B = 470\,k\Omega$, $R_C = 2.2\,k\Omega$, $V_{CC} = 18\,V$, and the transistor has $h_{fe} = 100$. Determine I_B, I_C, and V_{CE}.

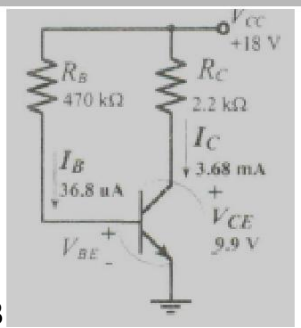


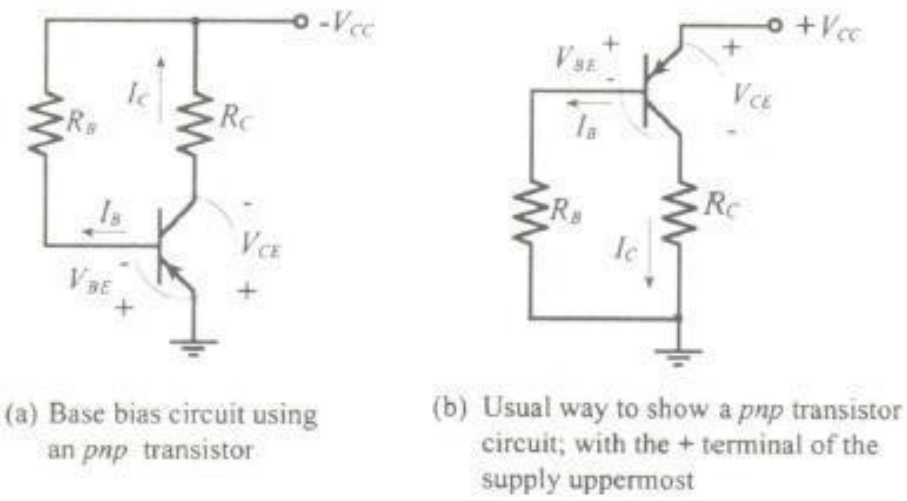
Fig-3.3

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\,V - 0.7\,V}{470\,k\Omega}$$
$$= 36.8\,\mu A$$

$$I_C = h_{fE} I_B = 100 \times 36.8\,\mu A$$
$$= 3.68\ mA$$
$$V_{CE} = V_{CC} - I_C R_C = 18\ V - (3.68\ mA \times 2.2\ k\Omega)$$
$$= 9.9\ V$$

Base bias using pnp transistor:

All of the base bias circuit discussed for npn is also applicable for pnp transistor except for polarities of voltage and currents. The figure shows the pnp transistor biasing circuit. Note that the voltage polarities and current directions are reversed compared to npn transistor base bias circuit. The KVL equations can be applied for analyzing the pnp transistors base bias circuit in exactly the same way as for npn circuits discussed above.



(a) Base bias circuit using an *pnp* transistor

(b) Usual way to show a *pnp* transistor circuit; with the + terminal of the supply uppermost

Fig : *Base bias circuits using pnp transistors.*

b)Collector to base bias circuit:

Circuit operation and analysis:

The *collector-to-base bias* circuit shown in Fig.5-17(a) has the base resistor R_B connected between the transistor collector and base terminals. As will be demonstrated. this circuit has significantly improvedbias stability for *hpE* changes compared to base bias. Refer to Fig. 5-17(b) and note that the voltage across *RB* is dependent on *VeE*•

$$V_{CE} = V_{BE} + I_B R_B$$

giving, $$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

Also, V_{CE} is dependent on the level of I_C and I_B,

$$V_{CE} = V_{CC} - R_C(I_C + I_B)$$

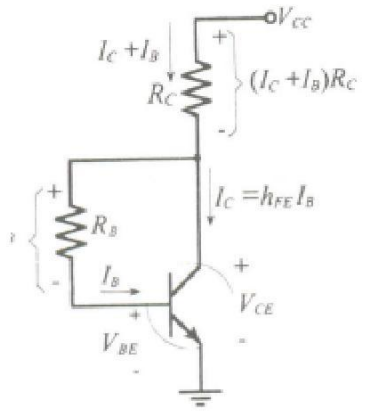


Fig 3.6: Collector-to-base bias circuits. Any change in V_{CE} changes I_B The I_B change causes I_C to change, and this tends to return I_C toward its original level.

***Note that the voltage across* $\mathbf{R_B}$. *is dependent on* $\mathbf{V_{CE}}$ *and* $\mathbf{V_{CE}}$ *is independent of the level of Ic and* $\mathbf{I_B}$.**

If Ic increases above the design level there is an increased voltage drop across Rc, resulting in a reduction in V_{CE}..The reduced Vce level causes I_B to be lower than its design level and because Ic= β Ib, the collector current is also reduced. Thus, an increase in Ic produces a feedback effect that tends to return Ic toward its original level. Similarly, reduction in Ic produces an increase in Vce which increase I_B, thus tending to increase Ic back to the original level.

Analysis of this circuit is a little more complicated than base bias analysis. To simplify the process an equation is first derived for the base current I_B.. Equating equations 1 and 2,

Hence, $V_{CE} = Vcc - Rc (I_B + Ic) = V_{BE} + I_B R_B$

$$I_B (Rc + R_B) + Ic\ Rc = Vcc - V_{BE}$$

Substituting $Ic = \beta I_B$ into the above equation

$$I_B(Rc + R_B) + \beta I_B Rc = Vcc - V_{BE}$$

This gives

$$I_B = \frac{Vcc - V_{BE}}{(\beta + 1)\,Rc + R_B} \quad \text{---------- 3}$$

Effect of β (max) and β (min) in collector to base bias circuit

In the collector to base bias circuit, the feed back from the collector from the collector to base reduces the effects of β spread values, due to transistor replacement etc. Thus collector to base

bias has greater stability than base bias for a given range of β values. This is illustrated in the following example.

It is important to note that, unlike the situation in a base bias circuit, the base current in a collector to base bias circuit does not remain constant, rather I_B compensates for I_C increase due to negative feed back provided by the base bias resistor R_B, even when the transistor β value is changed as illustrated in the following example.

Comparing the base bias and the collector to base bias circuits for Q point stabilization against β variations, it is seen that the Q points for the collector to bias circuit is clearly has greater stability against β spread value than base bias circuit.

Collector to base bias circuit using pnp transistor.

Collector to base bias circuit using pnp transistor. is illustrated in fig. below. Note that the voltage polarities and current directions are reversed compared to npn transistor collector to base bias circuit. This circuit can be analyzed in exactly the same way as the npn transistor circuit.

Voltage divider bias circuit

Circuit operation

Voltage divider bias also known as emitter current bias, is the most stable of the three basic transistor biasing circuits. A voltage divider bias circuit is shown in fig. below, and the current and voltage conditions through out the discussions are illustrated in fig.8. It is seen that there is an emitter resistor R_E connected in series with emitter, so that the total dc load in series with the transistor is (Rc+ R_E) and this resistance must be used when drawing the dc load line for the circuit. Resistor R1 and R2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage I_B.

Voltage divider bias circuits are normally designed to have the voltage divider current (I2) very much larger than the transistor base current (I_B).In this circumstance, V_{BE} is largely affected by I_B so V_{BE} can be assumed to remain constant.

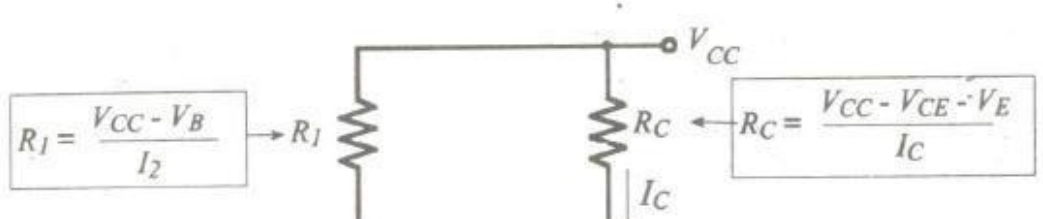


Fig. : Voltage divider bias circuit.

Referring to above figure 8, with V_B constant, the voltage across the emitter resistor is also a constant quantity; this means that the emitter current is constant,

The collector current is approximately equal to the emitter current, so Ic is held at constant level. Again referring to the figure, the transistor collector to emitter voltage is,

$$V_{CE} = Vcc - (I_C + I_B) R_C$$

Clearly, with Ic and I_E constant, the transistor collector- emitter voltage remains at a constant level. It should be noted that the transistor β value is not involved in any of the above equations.

The effect of max. and min. β in voltage divider bias circuit

The following example will demonstrate the variation of β with transistor replacements. The variations of β on the operating point Q is much less than the C-B bias. Hence this biasing technique is more reliable and stable. This makes it the most popular and preferred biasing technique used in circuits.

Comparison of varies biasing techniques.

a) Base bias circuit: The stability of this circuit is less. No feed back is used. Used only where stability is not important like switching circuits.
b) Collector to base bias: Moderately used, has moderate stability.Negetive feedback is used. It is used in switching applications where moderate stability is essential.

c) Widely used, has highest stability. Negative feedback is used .Due to excellent stability it is always the preferred circuit.

Stability factor-S

The stability factor S is defined as the rate of change of collector current with respect to the reverse saturation current, keeping β and V_{BE} constant.

$$S = \frac{\Delta I_C}{\Delta I_{CBO}}$$

or, $$\Delta I_C = S \times \Delta I_{CBO}$$

This definition facilitates the comparison of the stability provided by different biasing circuits. The minimum value of S=1, this means if Icbo increases say 1μA, then Ic also increases by 1μA.The value of S more likely the circuit will exhibit thermal instability, therefore the higher value of S is not favorable value of S<10 is considered good.

The general equation of $Ic=\beta I_B+(1+\beta)\ \beta I_{CBO}$

The general equation of Ic if we differentiate with respect to Ic with β as constant.

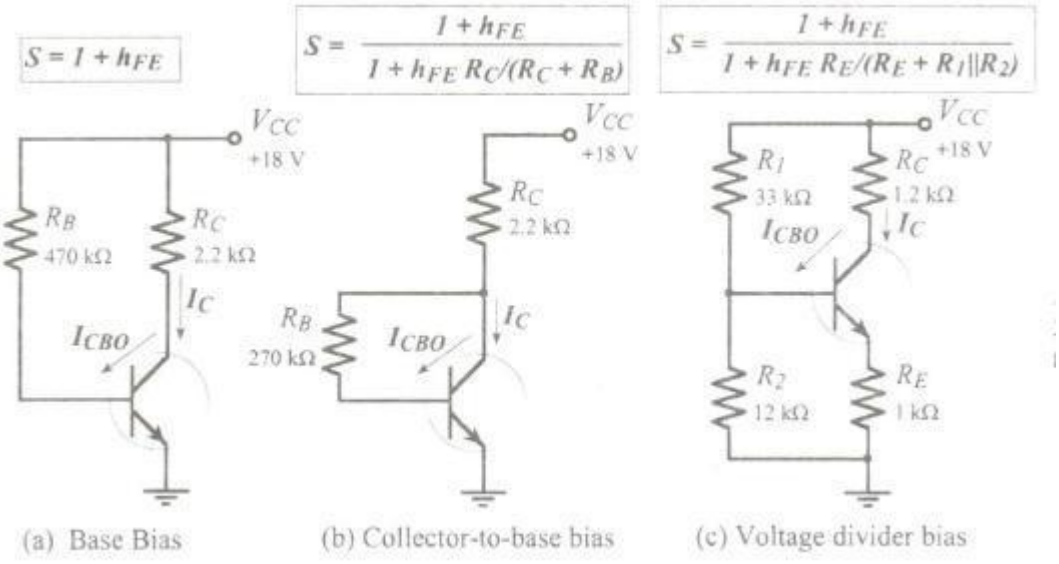
The stability factors for the three basic biasing circuits is shown below

For base bias,

$$S = 1 + h_{FE}$$

For collector-to-base bias,

$$S = \frac{1 + h_{FE}}{1 + h_{FE} R_C/(R_C + R_B)}$$



(a) Base Bias (b) Collector-to-base bias (c) Voltage divider bias

OPERATIONAL AMPLIFIER

Op-Amp (operational amplifier) is basically an amplifier available in the IC form. The word "operational" is used because the amplifier can be used to perform a variety of mathematical operations such as addition, subtraction, integration, differentiation etc.

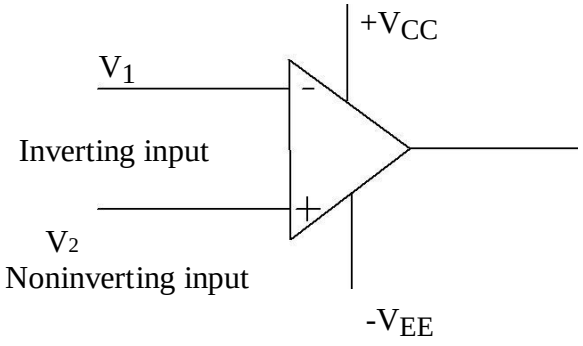


Fig. Symbol of Op-Amp

It has two inputs and one output. The input marked "-" is known as Inverting input and the input marked "+" is known as Non-inverting input.

- If a voltage V_i is applied at the inverting input (keeping the non-inverting input at ground) as shown below.

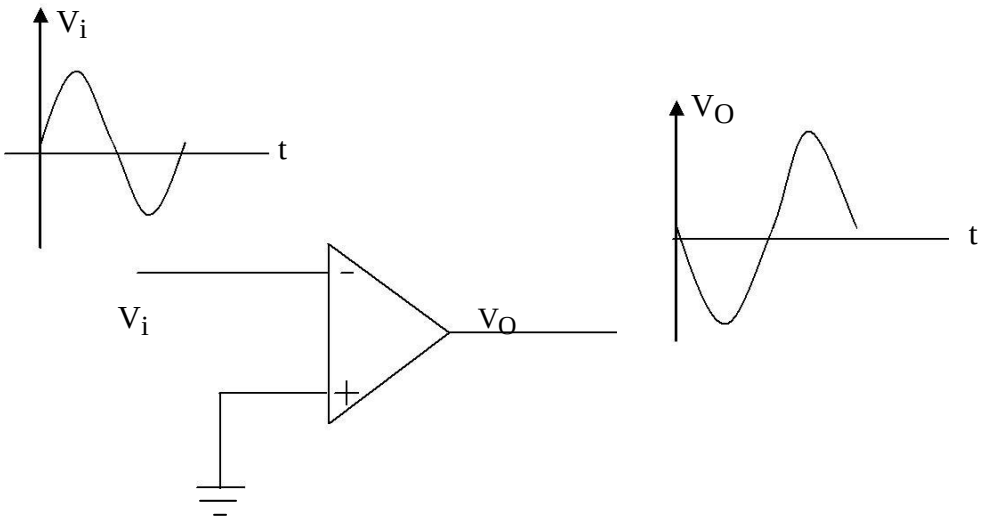


Fig. Op-amp in inverting mode

The output voltage $V_o = -AV_i$ is amplified but is out of phase with respect to the input signal by 180^0.

- If a voltage V_i is fed at the non-inverting input (Keeping the inverting input at ground) as shown below.

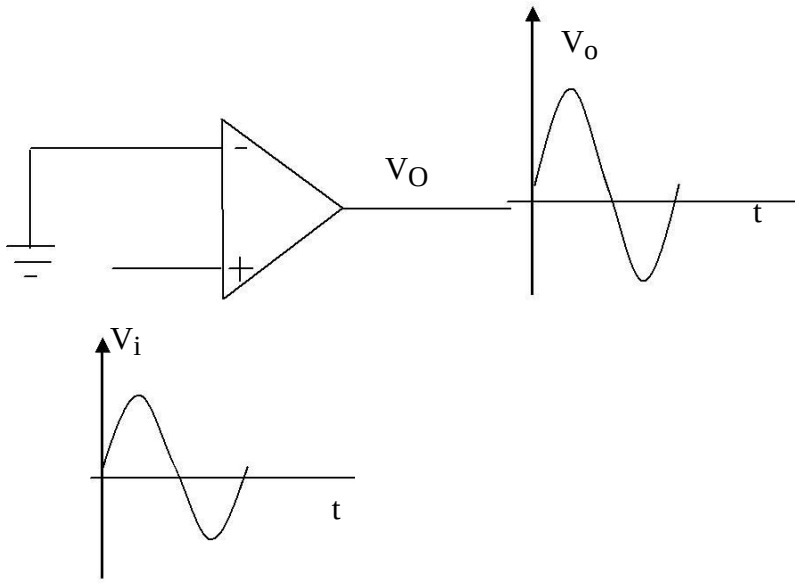


Fig. Op-Amp in Non-inverting mode

The output voltage $V_o = AV_i$ is amplified and in-phase with the input signal.

- If two different voltages V_1 and V_2 are applied to an ideal Op-Amp as shown below.

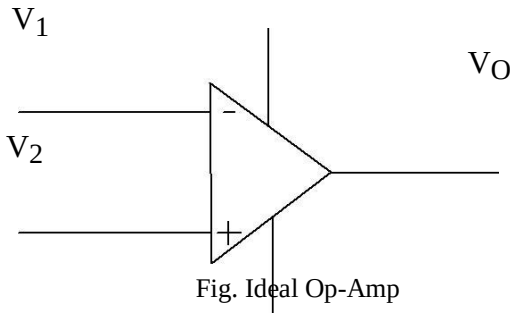


Fig. Ideal Op-Amp

The output voltage will be $V_o = A(V_1 - V_2)$

i.e the difference of the tow volatages is amplified. Hence an Op-Amp is also called as a High gain differential amplifier.

Note: Op-Amp is 8 pin IC (named as μA 741) with pin details as shown.

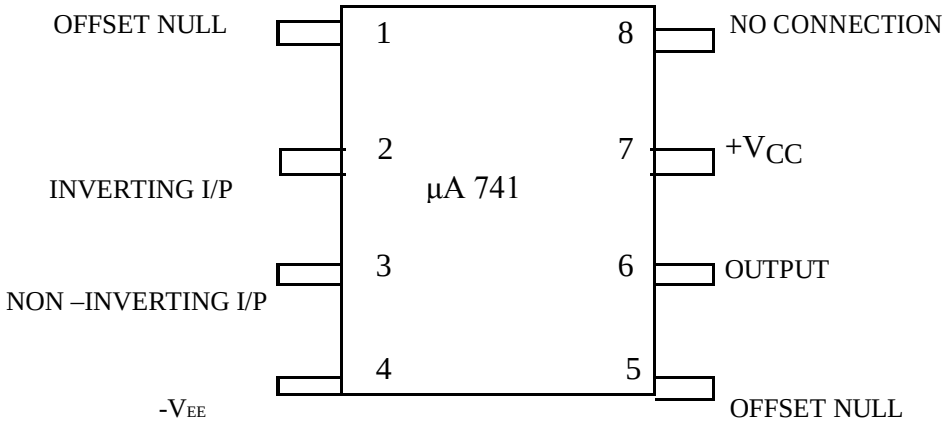


Fig. Pin details of Op-Amp

Block Diagram of an Op-AMP

An Op-Amp consists of four blocks cascaded as shown above

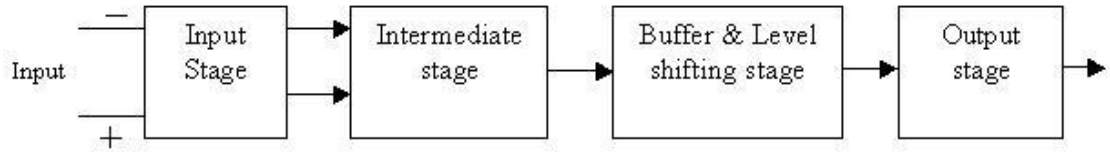


Fig. Block diagram of an Op-Amp

Input stage: It consists of a dual input, balanced output differential amplifier. Its function is to amplify the difference between the two input signals. It provides high differential gain, high input impedance and low output impedance.

Intermediate stage: The overall gain requirement of an Op-Amp is very high. Since the input stage alone cannot provide such a high gain. Intermediate stage is used to provide the required additional voltage gain.

It consists of another differential amplifier with dual input, and unbalanced (single ended) output

Buffer and Level shifting stage

As the Op-Amp amplifies D.C signals also, the small D.C. quiescent voltage level of previous

stages may get amplified and get applied as the input to the next stage causing distortion the final output.

Hence the level shifting stage is used to bring down the D.C. level to ground potential, when no signal is applied at the input terminals. Buffer is usually an emitter follower used for impedance matching.

Output stage- It consists of a push-pull complementary amplifier which provides large A.C. output voltage swing and high current sourcing and sinking along with low output impedance.

Concept of Virtual ground

We know that , an ideal Op-Amp has perfect balance (ie output will be zero when input voltages are equal).

Hence when output voltage $V_o = 0$, we can say that both the input voltages are equal ie $V_1 = V_2$.

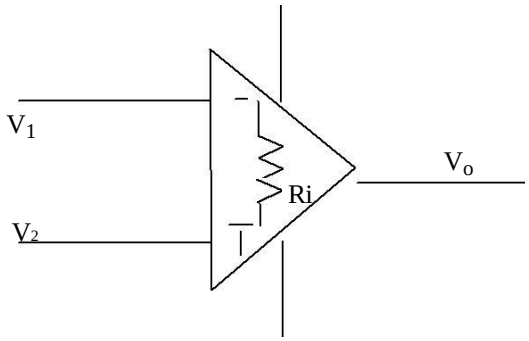


Fig. Concept of Virtual ground

Since the input impedances of an ideal Op-Amp is infinite (R_i =). There is no current flow between the two terminals.

Hence when one terminal (say V_2) is connected to ground (ie $V_2 = 0$) as shown.

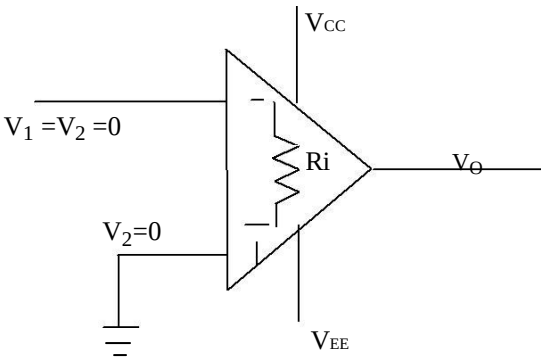


Fig. **Concept of Virtual ground**

Then because of virtual ground V_1 will also be zero.

Applications of Op-Amp

An Op-Amp can be used as

1. Inverting Amplifer
2. Non-Iverting Amplifer
3. Voltage follower
4. Adder (Summer)
5. Integrator
6. Differentiator

Definitions

1. **Slewrate(S):** It is defined as " The rate of change of output voltage per unit time"

$$s = \frac{dV_O}{dt} \qquad volts/\mu \text{ sec}$$

Ideally slew rate should be as high as possible.But its typical value is s=0.5 V/μ-sec.

2. **Common Mode Rejection Ratio(CMRR):** It is defined as " The ratio of differential voltage gain to common-mode voltage gain".

$$CMRR = \frac{A_d}{A_{CM}}$$

Ideally CMRR is infinite, but its typical value is CMRR = 90 dB

3. **Open Loop Voltage Gain (A_V):** It is the ration of output voltage to input voltage in the absence of feed back.

Its typical value is $A_V = 2x10^5$

4. **Input Impedance (R_i):**It is defined as " The impedance seen by the input(source) applied to one input terminal when the other input terminal is connected to ground.

Ri ≈ 2MΩ

5. **Output Impedance (R_O):** It is defined as " The impedance given by the output (load) for a particular applied input".

Ro ≈ 75Ω

Characteristics of an Ideal Op-Amp

An ideal Op-Amp has the following characteristics.

1. Infinite voltage gain (ie $A_V = \infty$)
2. Infinite input impedance ($R_{i=} \infty$)
3. Zero output impedance(R_o =0)
4. Infinite Bandwidth (B.W. = C
5. Infinite Common mode rejection ratio (ie CMRR =∞)
6. Infinite slew rate (ie S=∞)
7. Zero power supply rejection ratio (PSRR =0)ie output voltage is zero when power supply V_{CC} =0
8. Zero offset voltage(ie when the input voltages are zero, the output voltage will also be zero)
9. Perfect balance (ie the output voltage is zero when the input voltages at the two input terminals are equal)
10. The characteristics are temperature independent.

Inverting Amplifier

An inverting amplifier is one whose output is amplified and is out of phase by 180^0 with respect to the input

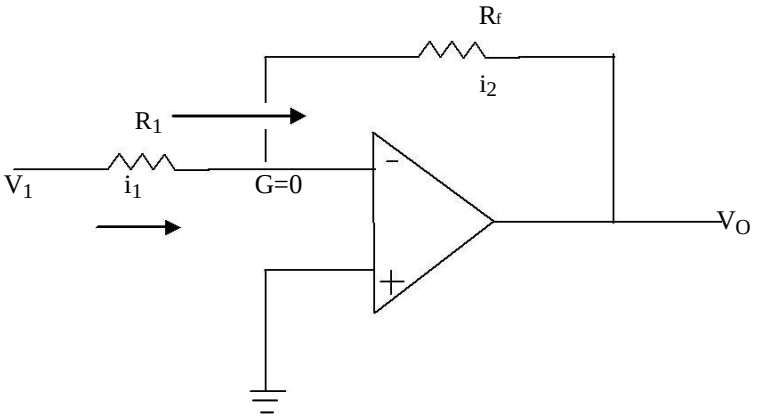


Fig:Inverting Amplifier

The point "G" is called virtual ground and is equal to zero.
By KCL we have

$$i_1 = i_2$$

$$\frac{V_i - 0}{R_1} = \frac{0 - V_o}{R_f}$$

$$\frac{V_i}{R_1} = -\frac{V_o}{R_f}$$

$$V_o = -\left(\frac{R_f}{R_1}\right) V_i$$

Where $\frac{R_f}{R_1}$ is the gain of the amplifier and negative sign indicates that the output is inverted with respect to the input.

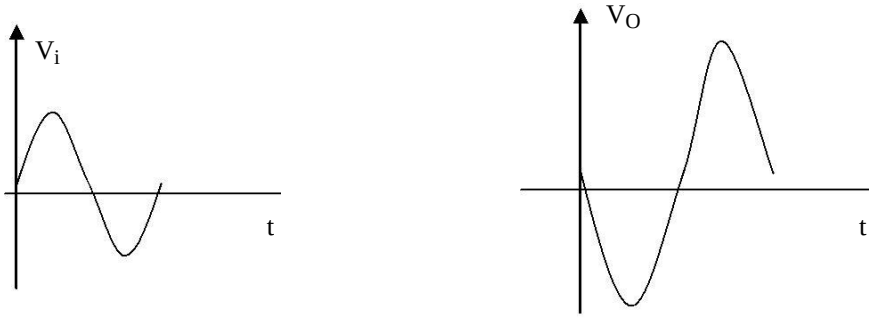


Fig. Waveforms of Inverting Amplifers

Non- Inverting Amplifier

A non-inverting amplifier is one whose output is amplified and is in-phase with the input.

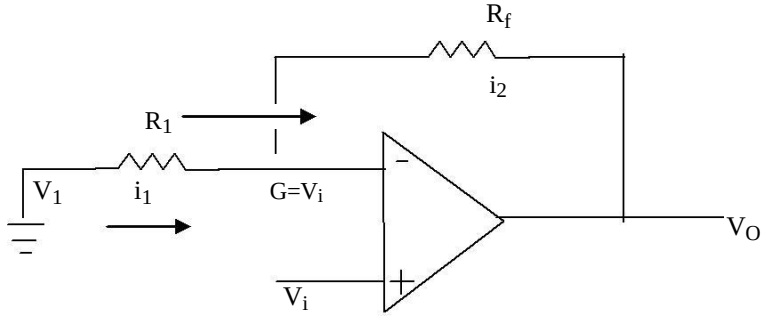


Fig. Non Inverting Amplifiers

By KCL we have

$$i_1 = -i_2$$

$$\frac{V_i - 0}{R_1} = -\frac{V_i - V_O}{R_f}$$

$$\frac{V_i}{R_1} = \frac{V_O - V_i}{R_f}$$

$$\frac{V_0 - Vi}{V_i} = \frac{R_f}{R_1}$$

$$\frac{V_o}{V_i} - 1 = \frac{R_f}{R_1}$$

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_i$$

Where $\left(1 + \frac{R_f}{R_1}\right)$ is the gain of the amplifier and + sign indicates that the output is in-phase with the input.

Voltage follower

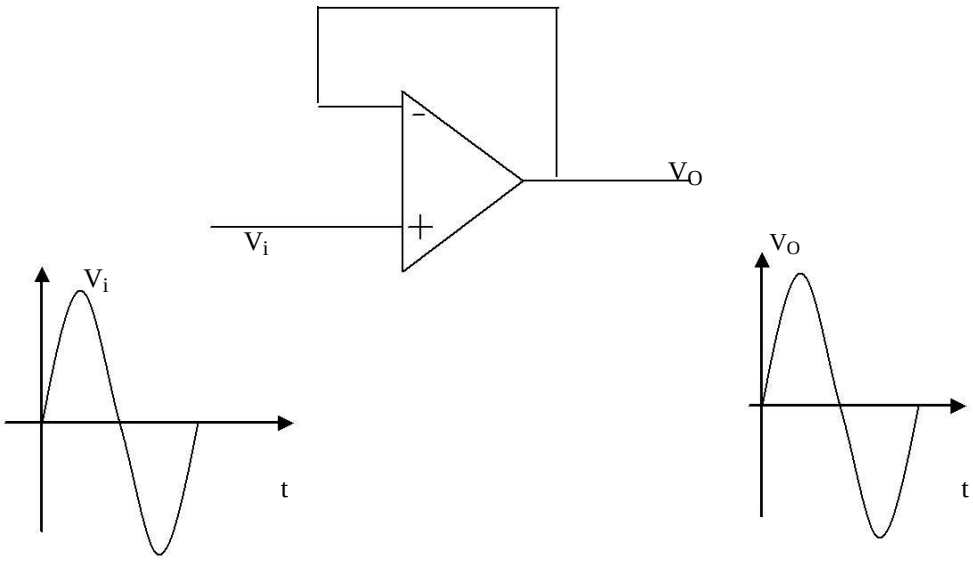


Fig. Voltage follower

Voltage follower is one whose output is equal to the input.

The voltage follower configuration shown above is obtained by short circuiting "R_f" and open circuiting "R_1" connected in the usual non-inverting amplifier.

thus all the output is fed back to the inverting input of the op-Amp.
Consider the equation for the output of non-inverting amplifer

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_i$$

When $R_f = 0$ short circuiting
$R_1 = \infty$ open circuiting

$$V_O = \left(1 + \frac{0}{\infty}\right) V_i$$

$$\therefore V_O = V_i$$

Therefore the output voltage will be equal and in-phase with the input voltage. Thus voltage follower is nothing but a non-inverting amplifier with a voltage gain of unity.

Inverting Adder

Inverting adder is one whose output is the inverted sum of the constituent inputs

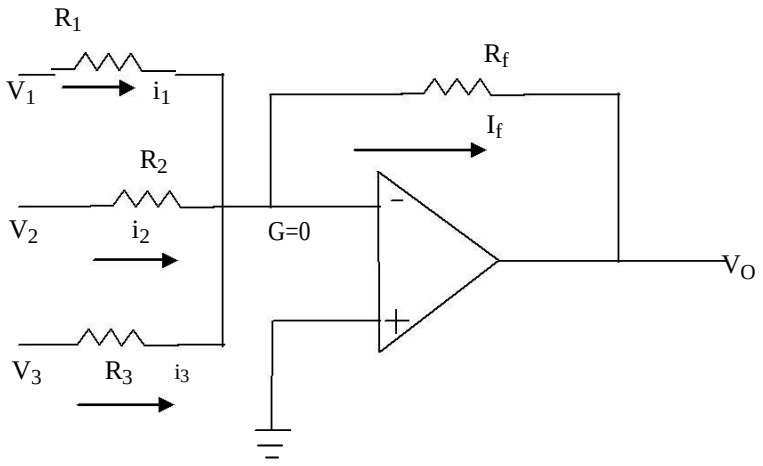


Fig.6.12. Inverting Adder

By KCL we have

$$i_f = i_1 + i_2 + i_3$$

$$\frac{0 - V_O}{R_f} = \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3}$$

$$\frac{V_O}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_O = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

If $R_1 = R_2 = R_3 = R$ then

$$V_O = -\frac{R_f}{R}\left[V_1 + V_2 + V_3\right]$$

If $R_f = R$ then

$V_O = -[V_1 + V_2 + V_3]$

Hence it can be observed that the output is equal to the inverted sum of the inputs.

Integrator

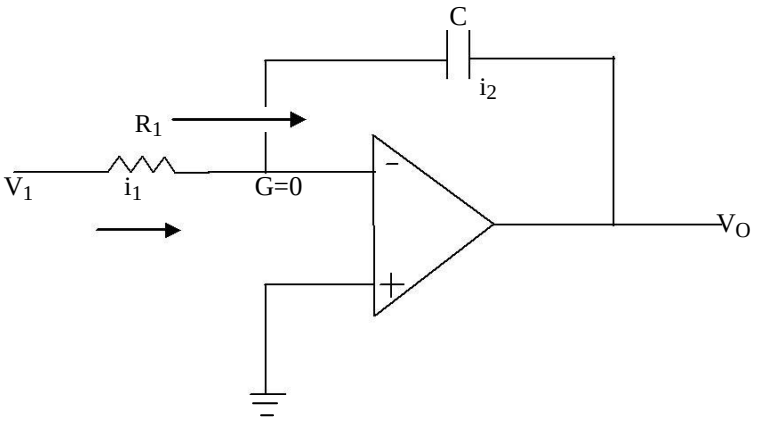


Fig:Integrator

An integrator is one whose output is the integration of the input.,

By KCL we have,

$$i_1 = i_2 \text{ ----------1}$$

From the above figure we have

$$i_1 = \frac{V_i - 0}{R} = \frac{V_i}{R} \text{ ----------2}$$

and similarly we have

$$0 - V_O = \frac{1}{C}\int i_2\, dt$$

$$V_O = -\frac{1}{C}\int i_2\, dt$$

$$\frac{dV_O}{dt} = -\frac{1}{C} i_2$$

$$i.e.\ i_2 = -C \frac{dV_O}{dt} \text{ ----------3}$$

substituin g 2 and 3 in 1 we have

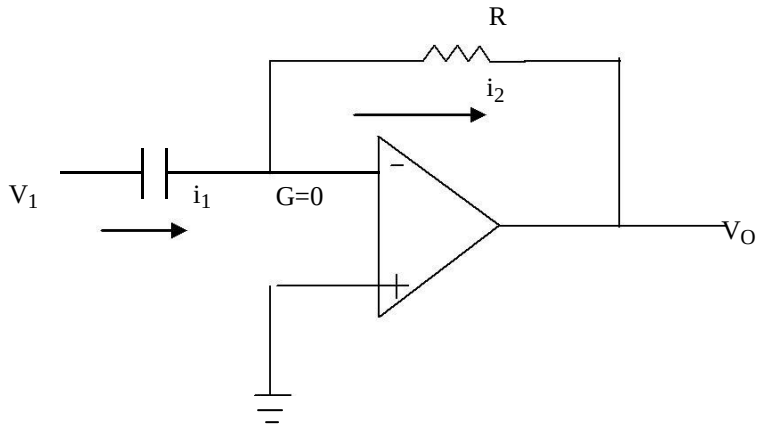
$$\frac{V_i}{R} = -C \frac{dV_O}{dt}$$

$$\frac{dV_O}{dt} = -\frac{1}{RC} V_i$$

$$\therefore V_O = -\frac{1}{RC}\int V_i\, dt$$

Differentiator

A differentiator is one whose output is the differentiation of the input



By KCL we have

$i_1 = i_2$ ----------1

From the above figure we have

$$V_i = \frac{1}{C}\int i_1\,dt$$

$$\frac{dV_i}{dt} = \frac{1}{C} i_1$$

$$i_1 = C.\frac{dV_i}{dt}$$ ---------- 2

and similarly we have

$$i_2 = \frac{0 - V_O}{R} = -\frac{V_O}{R}$$ ---------- 3

substituting 2 *and* 3 *in* 1 *we have*

$$C\frac{dV_i}{dt} = -\frac{V_O}{R}$$

$$V_O = -RC\frac{dV}{dt}$$

MODLUE-3

DIGITAL ELECTRONICS

The human need to count things goes back to the dawn of civilization. To answer the questions like "how much", or "how many", people invented number system. A number system is any scheme used to count things. The decimal number system succeeded because very large numbers can be expressed using relatively short series of easily memorized numerals. Decimal or base 10 number system's origin: can be traced to, counting on the fingers with digits. "Digit" taken from the Latin word *digitus* meaning "finger"

In any number system, the important terms to be known are :

Base or radix, numerals, positional value, absolute value, radix point and the prevalent number systems of interest for study.

Base: Base is the number of different digits or symbols or numerals used to represent the number system including zero in the number system. It is also called the **radix** of the number system.
Numeral : Numeral is the symbols used to represent the number system

Each digit in the number system has two values:

a) *Absolute value*
b) *Positional value*

The **absolute value** is the value of the digit itself, representing the no. system. The **positional value** is the value it possesses by virtue of its position in the no. system

The different number systems of interest for study, from the point of view of application to computers are:

Examples of commonly used number systems :

- **decimal**
- **binary**
- **octal**
- **hexadecimal**.

Important properties of these systems need to be studied.

Polynomial Notation **(Series Representation) :**Any number system can be represented by the following polynomial.

$$N = a_{n-1} \times r^{n-1} + a_{n-2} \times r^{n-2} + .. + a_0 \times r^0 + a_{-1} \times r^{-1} ... + a_{-m} \times r^{-m}$$

Where ***r*** **= radix or base**

n **= number of integer digits to the left of the radix point**

m **= number of fractional digits to the right of the radix point** ***an-1*** **= most significant digit (MSD)**

a-m **= least significant digit (LSD)**

Example:

$$N = (251.41)_{10} = 2 \times 10^2 + 5 \times 10^1 + 1 \times 10^0 + 4 \times 10^{-1} + 1 \times 10^{-2}$$

Decimal number system :

The decimal system is composed of 10 numerals or symbols. These 10 symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. Using these symbols as digits of a number, we can express any quantity. The decimal system is also called the base-10 system because it has 10 digits.
In decimal system, the no. 1000.111 is represented as:

← Integer part				→ ←	Fractional part →		
10^3	10^2	10^1	10^0		10^{-1}	10^{-2}	10^{-3}
=1000	=100	=10	=1	.	=0.1	=0.01	=0.001
Most Significant Digit				Decimal point			Least Significant Digit

Example : Multiply the value of the ***symbol*** by the value of the ***position***, then add
In decimal, 1954.89means

1 times 1,000
plus 9 times 100
plus 5 times 10
plus 4 times 1
plus 8 times 1/10

plus 9 times 1/100 = The number is 1954.89 in decimal. and is represented by $(1954.89)_{10}$. The digits are separated by a point **"."** called the radix point. In decimal system it is called "decimal point".

- 14_{10}
- 52_{10}
- 1024_{10}
- 64000_{10}

Binary number system :

In the binary system, there are only two symbols or possible digit values, 0 and 1. This base-2 system can be used to represent any quantity that can be represented in decimal or other base system.

← Integer part				→ ←	Fractional part →		
2^3	2^2	2^1	2^0		2^{-1}	2^{-2}	2^{-3}
=8	=4	=2	=1	.	=0.5	=0.25	=0.125
Most Significant Digit				Binary point			Least Significant Digit

Binary Counting

The Binary counting sequence to represent decimal numbers is shown in the table below :

2^3	2^2	2^1	2^0	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Representing Binary Quantities

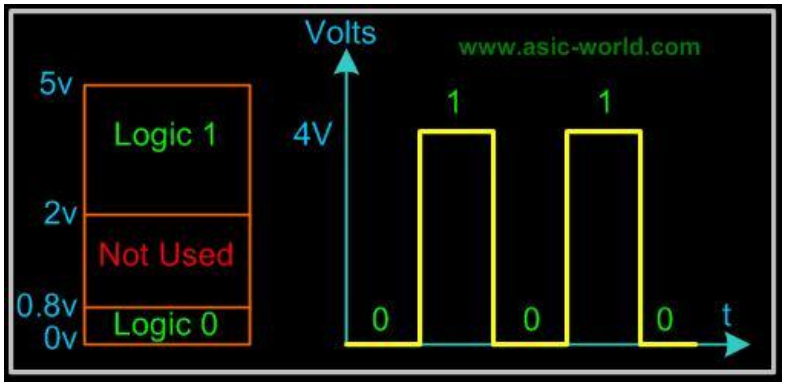
In digital systems the information that is being processed is usually presented in binary form. Any device that has only two operating states or possible conditions can represent binary quantities. E.g.. a switch which can be either be only open or closed. We arbitrarily (as we define them) let

an open switch represent binary 1 and a closed switch represent binary 0. Thus we can represent any binary number by using series of switches.

Typical Voltage Assignment

Binary 1: Any voltage between 2V to 5V
Binary 0: Any voltage between 0V to 0.8V

Not used: Voltage between 0.8V to 2V in 5 Volt CMOS and TTL Logic is not used as it may



cause error in a digital circuit.

We can see another significant difference between digital and analog systems. In digital systems, the exact voltage value is not important; eg, a voltage of 3.6V means the same as a voltage of 4.3V. In analog systems, the exact voltage value is important

Binary addition and subtraction: Examples of addition and subtraction in this number system is shown below:

The addition of binary numbers is done as follows:

a) 1 + 1 = 0 with a carry of 1, and can be represented as $(10)_2$, with 0 taking LSD position and 1 taking MSD.
b) 1 + 0 = 1
c) 0 + 1 = 1
d) 0 + 0 = 0

Example: Add the binary numbers 101011 and 11001

Sol: The binary addition process is indicated below,

Addition

111011 Carries ← the carries generated during addition is indicated here.

101011 Augend

+ 11001 Addend

1000100

The answer is : **$(101011)_2 + (11001)_2 = (1000100)_2$**

The subtraction of binary numbers is done as follows:

e) 1 - 1 = 0
f) 1 - 0 = 1
g) 0 - 1 = 0 with a barrow of 1 from previous stage
h) 0 - 0 = 0

Example: Subtract the binary numbers 11011 from100101.

Sol: The binary subtraction process is indicated below,

Subtraction

0 1 10 0 10 Borrows ← the barrows taken during subtraction is indicated here.
1 0 0 1 01 Minuend
1 1 0 11 Subtrahend
0 1 0 10

The answer is : **$(100101)_2 - (11011)_2 = (01010)_2$**

Octal Number System

The octal number system has a base of eight, meaning that it has eight possible digits: 0,1,2,3,4,5,6,7.

8^3	8^2	8^1	8^0		8^{-1}	8^{-2}	8^{-3}
=512	=64	=8	=1	.	=1/8	=1/64	=1/512

The octal numbering system includes eight base digits (0-7).After 7, the next placeholder to the right begins with a "1"
0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13 ...

Octal to Decimal Conversion

- $237_8 = 2 \times (8^2) + 3 \times (8^1) + 7 \times (8^0) = 159_{10}$
- $24.6_8 = 2 \times (8^1) + 4 \times (8^0) + 6 \times (8^{-1}) = 20.75_{10}$
- $11.1_8 = 1 \times (8^1) + 1 \times (8^0) + 1 \times (8^{-1}) = 9.125_{10}$
- $12.3_8 = 1 \times (8^1) + 2 \times (8^0) + 3 \times (8^{-1}) = 10.375_{10}$

Procedure :
Addition of first column 1+4= 5
Addition of second column 7+5= 12 and 12-8 = 4, with a carry of 1 to left
Addition of third column 1+4+7= 12 and 12-8 = 4, with a carry of 1 to left
Addition of fourth column 1+5+3= 9 and 9-8 = 1, with a carry of 1 to left
The final carry forms the MSD.
The answer is : **$(5471)_8 + (3754)_8 = (11445)_8$**

Subtraction

Example: Subtract the octal numbers 7451 and 5643
Sol : The subtraction process with procedure is shown below :

6 10 4 10 Borrows ← **the barrows taken during subtraction is indicated here.**

7 4 5 1 Minuend
- 5 6 4 3 Subtrahend
1 6 0 6 Difference

Procedure :

Subtraction of first column 1-3= 6,by borrowing carry from previous stage 1+8= 9, hence 9-3=6

Subtraction of second column 4-4= 0,now after the barrow 5 becomes 4 in II column.
Subtraction of third column 4-6= 6, by borrowing from previous stage, 8+4=12,
Hence 12-6 = 6

Subtraction of fourth column 6-5= 1, 7 will become 6 after a barrow to the right. The answer is : **$(7451)_8 - (5643)_8 = (1606)_8$**

Hexadecimal number system

The hexadecimal system uses base 16. Thus, it has 16 possible digit symbols. It uses the digits 0 through 9 plus the letters A, B, C, D, E, and F ,to represent 10 through 16, as the 16 digit symbols

Digits = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F}

$$(B65F)_{16} = 11 \times 16^3 + 6 \times 16^2 + 5 \times 16^1 + 15 \times 16^0 = (46,687)_{10}$$

- **Sometimes, it is necessary to use a numbering system that has more than ten base digits**
- **One such numbering system is hexadecimal number system, useful in computer application.**
- **Hexadecimal number, is widely used in micro processors and micro controllers in assembly programming, and in embedded system development.**

Conversion of number systems.

Converting from one no. system to another is called conversion of no. system or code conversion, like converting from binary to decimal or converting from hexadecimal to decimal etc.The possibilities of conversions of above number system is shown below.

Binary-To-Decimal Conversion

The binary number system is the most important one in digital systems, but several others are also important. The decimal system is important because it is universally used to represent quantities outside a digital system. This means that there will be situations where decimal values have to be converted to binary values before they are entered into the digital system.

Any binary number can be converted to its decimal equivalent simply by summing together the weights of the various positions in the binary number which contain a

together the weights of the various positions in the binary number which contain a 1.

Technique

- **Multiply each bit by 2^n, where *n* is the "weight" of the bit**
- **The weight is the position of the bit, starting from 0 on the right**
- **Add the results**

Example:

Binary	Decimal
10110101_2	
$2^7+0^6+2^5+2^4+0^3+2^2+0^1+2^0$	=128+0+32+16+0+4+0+1
Result	181_{10}

You should have noticed that the method is to find the weights (i.e., powers of 2) for each bit position that contains a 1, and then to add them up.

Binary to decimal Fractions:
Example :

10.1011 => $1 \times 2^{-4} = 0.0625$
$1 \times 2^{-3} = 0.125$
$0 \times 2^{-2} = 0.0$
$1 \times 2^{-1} = 0.5$
$0 \times 2^{0} = 0.0$
$1 \times 2^{1} = 2.0$
=2.6875

Procedure: Same principles with following exception ;.

Use negative powers of the base to the right of the radix point. (Only call it a decimal point in the decimal number system.)

Decimal-To-Binary Conversion

There are 2 methods:

- Reverse of Binary-To-Decimal Method
- Repeat Division

Reverse of Binary-To-Decimal Method

Example :

Decimal	Binary
45_{10}	=32 + 0 + 8 + 4 +0 + 1
	$=2^5+0+2^3+2^2+0+2^0$
Result	$=101101_2$

Repeat Division-Convert decimal to binary

This method uses repeated division by 2.

Example :

Conversion of 27_{10} to binary

Division	Remainder	Binary
25/2	= 12+ remainder of 1	1 (Least Significant Bit)
12/2	= 6 + remainder of 0	0
6/2	= 3 + remainder of 0	0
3/2	= 1 + remainder of 1	1
1/2	= 0 + remainder of 1	1 (Most Significant Bit)
Result	25_{10}	= 11001_2

Procedure :

Divide by two, keep track of the remainder

Group the remainders in the following order

First remainder is bit LSB (least-significant bit)
Last remainder is bit MSB (Most-significant bit)

Binary-To-Octal / Octal-To-Binary Conversion

Octal Digit	0	1	2	3	4
Binary Equivalent	000	001	010	011	100

Each Octal digit is represented by three binary digits.

Example: $100\ 111\ 010_2 = (100)\ (111)\ (010)_2 = 4\ 7\ 2_8$

Octal to decimal

5	6	7
101	110	111

Procedure

- **Multiply each bit by 8^n, where *n* is the "weight" of the bit**
- **The weight is the position of the bit, starting from 0 on the right Add**
- **the results.**

Example:

724.25_8 => $4 \times 8^0 = 4$

$2 \times 8^1 = 16$

$7 \times 8^2 = 448$

$2 \times 1/8 = 0.25$

$5 \times 1/8^2 = 0.015625$

Ans: $724_8 = 468.265625_{10}$

Decimal to octal

Repeat Division-Convert decimal to octal : This method uses repeated division by 8.

Example: Convert 177_{10} to octal and binary

Division	Result	Binary
177/8	= 22+ remainder of 1	1 (Least Significant Bit)
22/ 8	= 2 + remainder of 6	6
2 / 8	= 0 + remainder of 2	2 (Most Significant Bit)
Result	177_{10}	$= 261_8$
Binary		$= 010110001_2$

Hexadecimal to Decimal/Decimal to Hexadecimal Conversion

Example: $2AF_{16} = 2 \times (16^2) + 10 \times (16^1) + 15 \times (16^0) = 687_{10}$

Hexadecimal to Decimal Conversion

Technique

- **Multiply each bit by 16^n, where *n* is the "weight" of the bit**
- **The weight is the position of the bit, starting from 0 on the right**
- **Add the results**

Example:

$ABC.6D_{16}$ => C x 16^0 = 12 x 1 = 12

B x 16^1 = 11 x 16 = 176

A x 16^2 = 10 x 256 = 2560

6 x 1/16 = 6 x .0625

D x 1/16^2 = 13 x .0039

= 2748.0664_{10}

Ans: ABC_{16} = 2748.0664_{10}

- $24.6_{16} = 2 \times (16^1) + 4 \times (16^0) + 6 \times (16^{-1}) = 36.375_{10}$
- $11.1_{16} = 1 \times (16^1) + 1 \times (16^0) + 1 \times (16^{-1}) = 17.0625_{10}$
- $12.3_{16} = 1 \times (16^1) + 2 \times (16^0) + 3 \times (16^{-1}) = 18.1875_{10}$

Decimal To Hexadecimal

Repeat Division- Convert decimal to hexadecimal - This method uses repeated division by 16.

Example: convert 378_{10} to hexadecimal and binary:

Division	Result	Hexadecimal
378/16	= 23+ remainder of 10	A (Least Significant Bit)23
23/16	= 1 + remainder of 7	7
1/16	= 0 + remainder of 1	1 (Most Significant Bit)
Result	378_{10}	= $17A_{16}$
Binary		= $0001\ 0111\ 1010_2$

Binary-To-Hexadecimal /Hexadecimal-To-Binary Conversion

Hexadecimal Digit	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Binary Equivalent	0000	0001	0010	0011	0100	0101	0110	0111
Hexadecimal Digit	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
Binary Equivalent	1000	1001	1010	1011	1100	1101	1110	1111

Each Hexadecimal digit is represented by **four** bits of binary digit

Example: $1011\ 0010\ 1111_2 = (1011)\ (0010)\ (1111)_2 = B\ 2\ F_{16}$

Octal-To-Hexadecimal, Hexadecimal-To-Octal Conversion

- Convert Octal (Hexadecimal) to Binary first.
- Regroup the binary number by three bits per group starting from LSB if Octal is required.
- Regroup the binary number by four bits per group starting from LSB if Hexadecimal is required

Example:
Convert 5A816 to Octal.

Hexadecimal	Binary/Octal
5A816	= **0101** 1010 **1000** (Binary)
	= **010** 110 **101** 000 (Binary)
Result	= 2 6 5 0 (Octal)

BOOLEAN ALGEBRA

Symbolic Logic

Boolean algebra derives its name from the mathematician George Boole. Symbolic Logic uses values, variables and operations

- **True** is represented by the value **1**.
- **False** is represented by the value **0**.:

Variables are represented by letters and can have one of two values, either 0 or 1. Operations are functions of one or more variables

- **AND** is represented by X.Y
- **OR** is represented by X + Y
- **NOT** is represented by X' . Throughout this tutorial the X' form will be used and sometime !X will be used.

These basic operations can be combined to give expressions

- **Example :** X
- X.Y
- W.X.Y + Z

Precedence

As with any other branch of mathematics, these operators have an order of precedence. NOT operations have the highest precedence, followed by AND operations, followed by OR operations. Brackets can be used as with other forms of algebra. e.g.

X.Y + Z and **X.(Y + Z)** are not the same function

Function Definitions

The logic operations given previously are defined as follows :

Define f(X,Y) to be some function of the variables X and Y.

f(X,Y) = X.Y

f(X,Y) = X.Y

- 1 if X = 1 and Y = 1
- 0 Otherwise

f(X,Y) = X + Y

- 1 if X = 1 or Y = 1
- 0 Otherwise

f(X) = X'

- 1 if X = 0
- 0 Otherwise

Truth Tables

Truth tables are a means of representing the results of a logic function using a table. They are constructed by defining all possible combinations of the inputs to a function, and then calculating the output for each combination in turn. For the three functions we have just defined, the truth tables are as follows

AND

X	Y	F(X,Y)
0	0	0
0	1	0
1	0	0
1	1	1

OR

X	Y	F(X,Y)
0	0	0
0	1	1
1	0	1
1	1	1

NOT

X	F(X)
0	1
1	0

Truth tables may contain as many input variables as desired

F(X,Y,Z) = X.Y + Z

X	Y	Z	F(X,Y,Z)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1

Boolean Switching Algebras

A Boolean Switching Algebra is one which deals only with two-valued variables. Boole's general theory covers algebras which deal with variables which can hold n values.

Identity :- X + 0 = X, X . 1 = X

Commutative Laws : X + Y = Y + X, X . Y = Y . X

Distributive Laws : X.(Y + Z) = X.Y + X.Z, X + Y.Z = (X + Y) . (X + Z)

Complement : X + X' = 1, X . X' = 0, The complement X' is unique.

Theorems: A number of theorems may be proved for switching algebras

Idempotent Law : X + X = X, X . X = X

DeMorgan's Law:

(X + Y)' = X' . ', These can be proved by the use of truth tables.

(X.Y) = X' + Y', These can be proved by the use of truth tables

Proof of (X.Y) = X' + Y'

X	Y	X.Y	(X.Y)'
0	0	0	1
0	1	0	1
1	0	0	1

X	Y	X'	Y'	X'+Y'
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

Note : DeMorgans Laws are applicable for any number of variables

Boundedness Law: X + 1 = 1: X . 0 = 0

Absorption Law : X + (X . Y) = X: X . (X + Y) = X

Elimination Law : X + (X' . Y) = X + Y, X.(X' + Y) = X.Y

Involution theorem : X" = X

Associative Properties : X + (Y + Z) = (X + Y) + Z, X . (Y . Z) = (X . Y) . Z

Duality Principle : In Boolean algebras the duality Principle can be obtained by interchanging AND and OR operators and replacing 0's by 1's and 1's by 0's. Compare the identities on the left side with the identities on the right.

Example : X.Y+Z' = (X'+Y').Z

It states that for every Boolean expression there exists another expression such that the anding is replaced by oring,and oring is replaced by anding, and all 0's are replaced by 1's and all 1's are replaced by 0's in the original expression.

Consensus theorem : X.Y + X'.Z + Y.Z = X.Y + X'.Z

or dual form as below, (X + Y).(X' + Z).(Y + Z) = (X + Y).(X' + Z)

Proof of X.Y + X'.Z + Y.Z = X.Y + X'.Z:

X.Y + X'.Z + Y.Z	**= X.Y + X'.Z**
X.Y + X'.Z + (X+X').Y.Z	= X.Y + X'.Z
X.Y.(1+Z) + X'.Z.(1+Y)	= X.Y + X'.Z
X.Y + X'.Z	= X.Y + X'.Z

X.Y'+Z).(X+Y).Z = X.Z+Y.Z instead of X.Z+Y'.Z

X.Y'Z+X.Z+Y.Z

(X.Y'+X+Y).Z

(X+Y).Z

X.Z+Y.Z

The term which is left out is called the consensus term

Given a pair of terms for which a variable appears in one term, and its complement in the other, then the consensus term is formed by AND ing the original terms together, leaving out the selected variable and its complement.

The consensus of X.Y and X'.Z is Y.Z

The consensus of X.Y.Z and Y'.Z'.W' is (X.Z).(Z.W')

Summary of Laws And Theorms

Identity	Dual
Operations with 0 and 1	
X + 0 = X (identity)	X.1 = X
X + 1 = 1 (null element)	X.0 = 0
Idempotency theorem	
X + X = X	X.X = X
Complementarity	
X + X' = 1	X.X' = 0
Involution theorem	
(X')' = X	
Cummutative law	
X + Y = Y + X	X.Y = Y X
Associative law	
(X + Y) + Z = X + (Y + Z) = X + Y + Z	(XY)Z = X(YZ) = XYZ
Distributive law	
X(Y + Z) = XY + XZ	X + (YZ) = (X + Y)(X + Z)
DeMorgan's theorem	
(X + Y + Z + ...)' = X'Y'Z'... or { f (X1,X2,...,Xn,0,1,+,.) } = { f (X1',X2',...,Xn',1,0,.,+) }	(XYZ...)' = X' + Y' + Z' + ...
Simplification theorems	
XY + XY' = X (uniting)	(X + Y)(X + Y') = X
X + XY = X (absorption)	X(X + Y) = X
(X + Y')Y = XY (adsorption)	XY' + Y = X + Y
Consensus theorem	
XY + X'Z + YZ = XY + X'Z	(X + Y)(X' + Z)(Y + Z) = (X + Y)(X' + Z)
Duality	
$(X + Y + Z + ...)^D$ = XYZ... or $\{f(X1,X2,...,Xn,0,1,+,.)\}^D$ = f(X1,X2,...,Xn,1,0,.,+)	$(XYZ ...)^D$ = X + Y + Z + ...

Logic Gates

A logic gate is an electronic circuit/device which makes the logical decisions. To arrive at this decisions, the most common logic gates used are OR, AND, NOT, NAND, and NOR gates. The

NAND and NOR gates are called universal gates. The exclusive-OR gate is another logic gate which can be constructed using AND, OR and NOT gate.

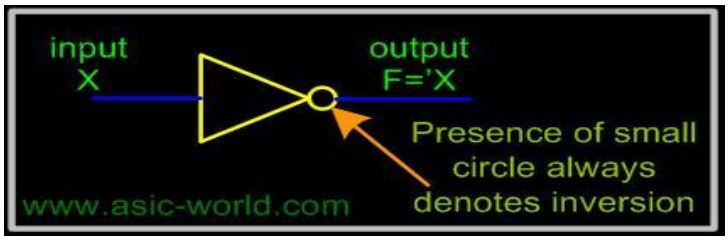
Logic gates have one or more inputs and only one output. The output is active only for certain input combinations. Logic gates are the building blocks of any digital circuit. Logic gates are also called switches. With the advent of integrated circuits, switches have been replaced by TTL (Transistor Transistor Logic) circuits and CMOS circuits. Here I give example circuits on how to construct simples gates.

Symbolic Logic

Boolean algebra derives its name from the mathematician George Boole. Symbolic Logic uses values, variables and operations.

Inversion

A small circle on an input or an output indicates inversion. See the NOT, NAND and NOR gates given below for examples.



Multiple Input Gates

Given commutative and associative laws, many logic gates can be implemented with more than two inputs, and for reasons of space in circuits, usually multiple input, complex gates are made. You will encounter such gates in real world (maybe you could analyze an ASIC lib to find this)

Gates Types

- AND
- OR
- NOT
- BUF

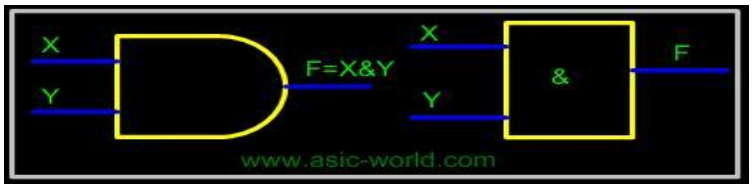
- NAND
- NOR
- XOR
- XNOR

AND Gate

The AND gate performs logical multiplication, commonly known as AND function. The AND gate has two or more inputs and single output. The output of AND gate is HIGH only when all its inputs are HIGH (i.e. even if one input is LOW, Output will be LOW).

If X and Y are two inputs, then output F can be represented mathematically as F = X.Y, Here dot (.) denotes the AND operation. Truth table and symbol of the AND gate is shown in the figure below.

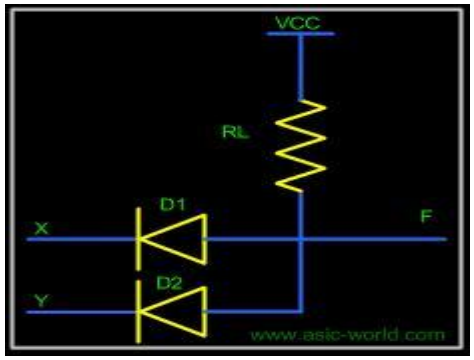
Symbol



Truth Table

X	Y	F=(X.Y)
0	0	0
0	1	0
1	0	0
1	1	1

Two input AND gate using "diode-resistor" logic is shown in figure below, where X, Y are inputs and F is the output.



If X = 0 and Y = 0, then both diodes D1 and D2 are forward biased and thus both diodes

conduct and pull F low.

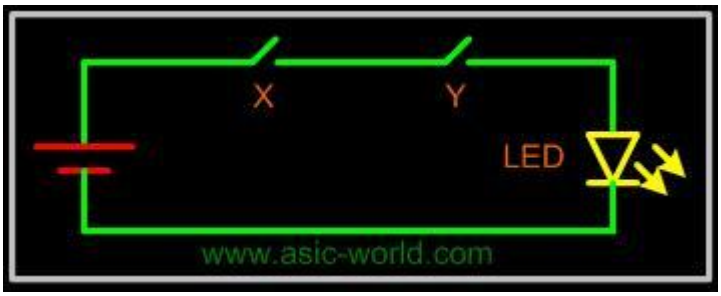
If X = 0 and Y = 1, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulls F low

If X = 1 and Y = 0, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulls F low.

If X = 1 and Y = 1, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus there is no drop in voltage at F. Thus F is HIGH.

Switch Representation of AND Gate

In the figure below, X and Y are two switches which have been connected in series (or just cascaded) with the load LED and source battery. When both switches are closed, current flows to LED.

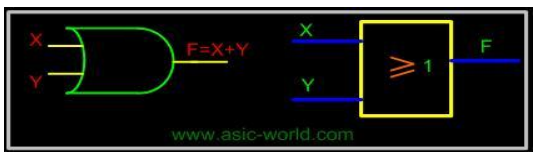


OR Gate

The OR gate performs logical addition, commonly known as OR function. The OR gate has two or more inputs and single output. The output of OR gate is HIGH only when any one of its inputs are HIGH (i.e. even if one input is HIGH, Output will be HIGH)

If X and Y are two inputs, then output F can be represented mathematically as F = X+Y. Here plus sign (+) denotes the OR operation. Truth table and symbol of the OR gate is shown in the figure below.

Symbol

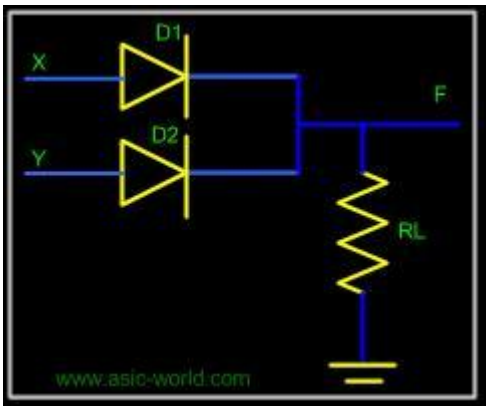


Truth Table

X	Y	F=(X+Y)
0	0	0
0	1	1
1	0	1
1	1	1

Two input OR gate using "diode-resistor" logic is shown in figure below, where X, Y are inputs and F is the output

Circuit



If X = 0 and Y = 0, then both diodes D1 and D2 are reverse biased and thus both the diodes are in cut-off and thus F is low

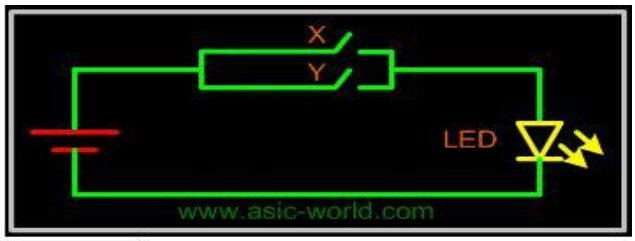
If X = 0 and Y = 1, D1 is reverse biased, thus does not conduct. But D2 is forward biased, thus conducts and thus pulling F to HIGH.

If X = 1 and Y = 0, D2 is reverse biased, thus does not conduct. But D1 is forward biased, thus conducts and thus pulling F to HIGH.

If X = 1 and Y = 1, then both diodes D1 and D2 are forward biased and thus both the diodes conduct and thus F is HIGH.

Switch Representation of OR Gate

In the figure, X and Y are two switches which have been connected in parallel, and this is connected in series with the load LED and source battery. When both switches are open, current does not flow to LED, but when any switch is closed then current flows.

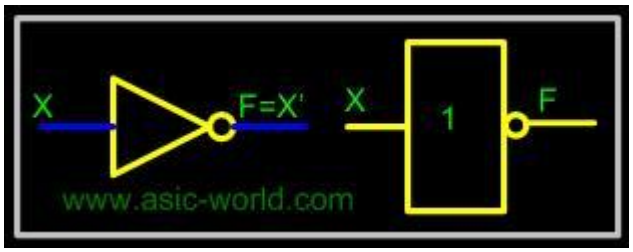


NOT Gate

The NOT gate performs the basic logical function called inversion or complementation. NOT gate is also called inverter. The purpose of this gate is to convert one logic level into the opposite logic level. It has one input and one output. When a HIGH level is applied to an inverter, a LOW level appears on its output and vice versa.

If X is the input, then output F can be represented mathematically as F = X', Here apostrophe (') denotes the NOT (inversion) operation. There are a couple of other ways to represent inversion, F= !X, here ! represents inversion. Truth table and NOT gate symbol is shown in the figure below

Symbol

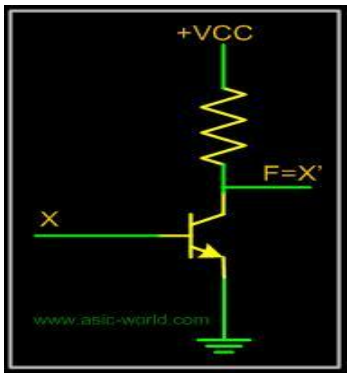


Truth Table

X	Y=X'
0	1
1	0

NOT gate using "transistor-resistor" logic is shown in the figure below, where X is the input and F is the output

Circuit



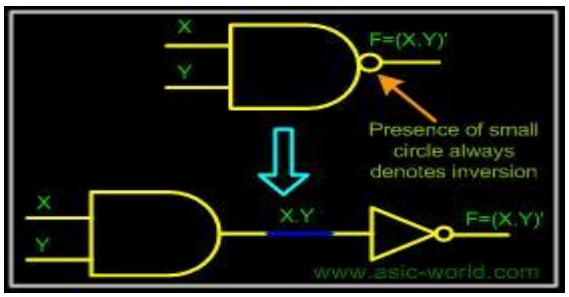
When X = 1, The transistor input pin 1 is HIGH, this produces the forward bias across the emitter base junction and so the transistor conducts. As the collector current flows, the voltage drop across RL increases and hence F is LOW.

When X = 0, the transistor input pin 2 is LOW: this produces no bias voltage across the transistor base emitter junction. Thus Voltage at F is HIGH.

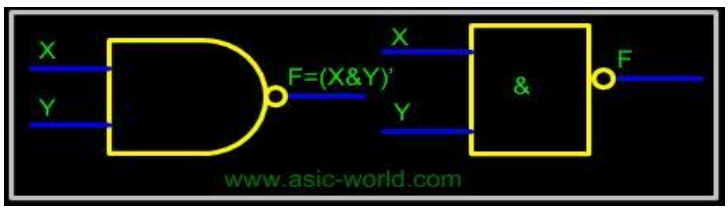
NAND Gate

NAND gate is a cascade of AND gate and NOT gate, as shown in the figure below. It has two or more inputs and only one output. The output of NAND gate is HIGH when any one of its input is LOW (i.e. even if one input is LOW, Output will be HIGH).

NAND From AND and NOT



If X and Y are two inputs, then output F can be represented mathematically as F = (X.Y)', Here dot (.) denotes the AND operation and (') denotes inversion. Truth table and symbol of the N AND gate is shown in the figure below. Symbol



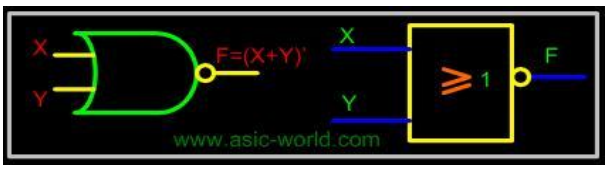
Truth Table

X	Y	F=(X.Y)'
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

NOR gate is a cascade of OR gate and NOT gate, as shown in the figure below. It has two or more inputs and only one output. The output of NOR gate is HIGH when any all its inputs are LOW (i.e. even if one input is HIGH, output will be LOW)

Symbol



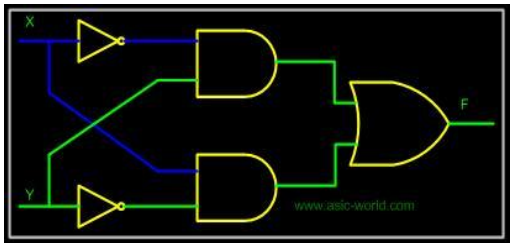
If X and Y are two inputs, then output F can be represented mathematically as F = (X+Y)'; here plus (+) denotes the OR operation and (') denotes inversion. Truth table and symbol of the NOR gate is shown in the figure below.

Truth Table

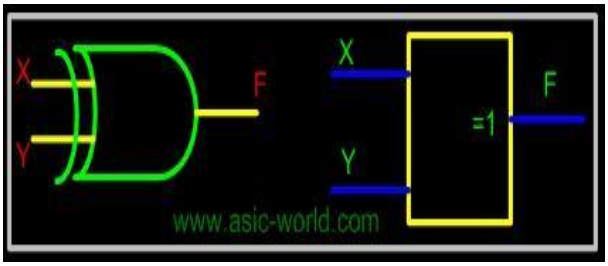
X	Y	F=(X+Y)'
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

An Exclusive-OR (XOR) gate is gate with two or three or more inputs and one output. The output of a two-input XOR gate assumes a HIGH state if one and only one input assumes a HIGH state. This is equivalent to saying that the output is HIGH if either input X or input Y is HIGH exclusively, and LOW when both are 1 or 0 simultaneously
If X and Y are two inputs, then output F can be represented mathematically as F = X⊕Y, Here ⊕ denotes the XOR operation. X⊕Y and is equivalent to X.Y' + X'.Y. Truth table and symbol of the XOR gate is shown in the figure below
XOR From Simple gates



Symbol



Truth Table

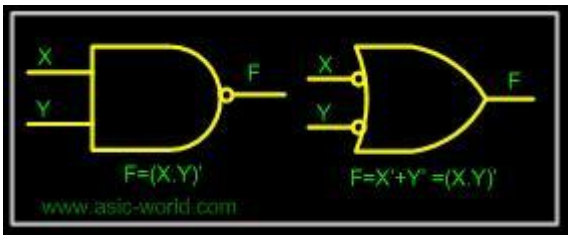
X	Y	F=(X Y)
0	0	0
0	1	1
1	0	1
1	1	0

Universal Gates

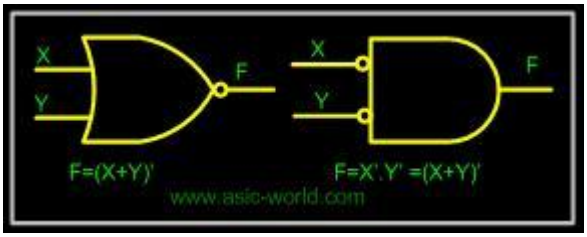
Universal gates are the ones which can be used for implementing any gate like AND, OR and NOT, or any combination of these basic gates; NAND and NOR gates are universal gates. But there are some rules that need to be followed when implementing NAND or NOR based gate

To facilitate the conversion to NAND and NOR logic, we have two new graphic symbols for these gates

NAND Gate



NOR Gate



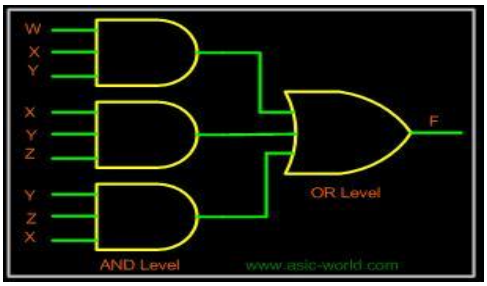
Realization of logic function using NAND gates

Any logic function can be implemented using NAND gates. To achieve this, first the logic function has to be written in Sum of Product (SOP) form. Once logic function is converted to SOP, then is very easy to implement using NAND gate. In other words any logic circuit with AND gates in first level and OR gates in second level can be converted into a NAND-NAND gate circuit.

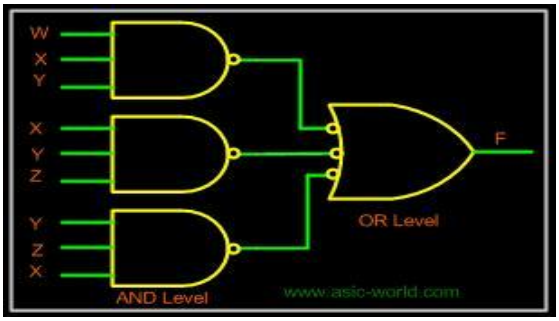
Consider the following SOP expression

F = W.X.Y + X.Y.Z + Y.Z.

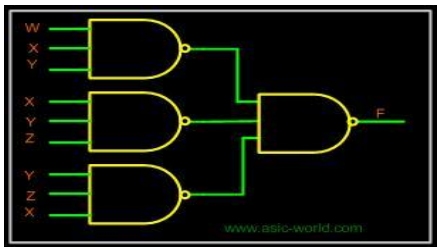
The above expression can be implemented with three AND gates in first stage and one OR gate in second stage as shown in figure



If bubbles are introduced at AND gates output and OR gates inputs (the same for NOR gates), the above circuit becomes as shown in figure



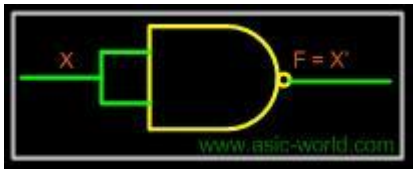
Now replace OR gate with input bubble with the NAND gate. Now we have circuit which is fully implemented with just NAND gates.



Realization of logic gates using NAND gates

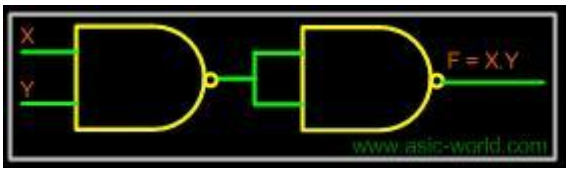
Implementing an inverter using NAND gate

Input	Output	Rule
(X.X)'	= X'	Idempotent



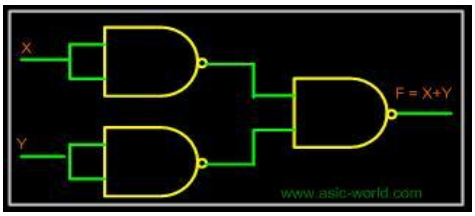
Implementing AND using NAND gates

Input	Output	Rule
((XY)'(XY)')'	= ((XY)')'	Idempotent
	= (XY)	Involution



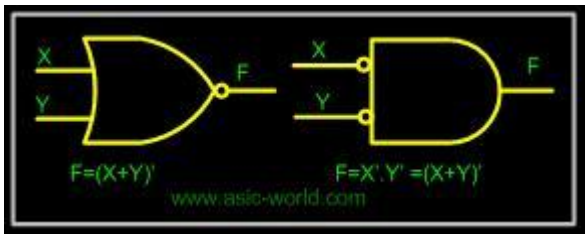
Implementing OR using NAND gates

Input	Output	Rule
((XX)'(YY)')'	= (X'Y')'	Idempotent
	= X"+Y"	DeMorgan
	= X+Y	Involution



Implementing NOR using NAND gates

Input	Output	Rule
((XX)'(YY)')'	=(X'Y')'	Idempotent
	=X"+Y"	DeMorgan
	=X+Y	Involution
	=(X+Y)'	Idempotent



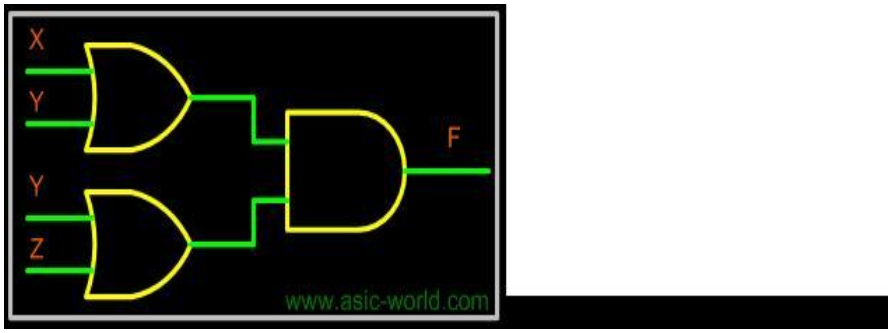
Realization of logic function using NOR gates

Any logic function can be implemented using NOR gates. To achieve this, first the logic function has to be written in Product of Sum (POS) form. Once it is converted to POS, then it's very easy to implement using NOR gate. In other words any logic circuit with OR gates in first level and AND gates in second level can be converted into a NOR-NOR gate circuit.

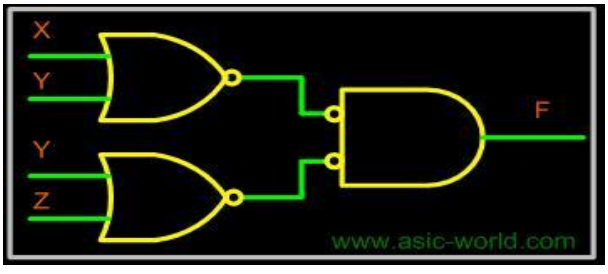
Consider the following POS expression

F = (X+Y) . (Y+Z)

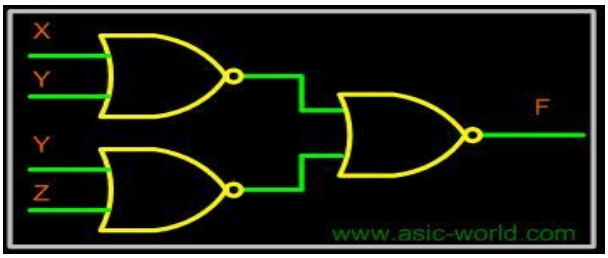
The above expression can be implemented with three OR gates in first stage and one AND gate in second stage as shown in figure.



If bubble are introduced at the output of the OR gates and the inputs of AND gate, the above circuit becomes as shown in figure.



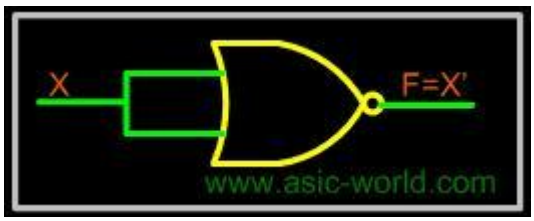
Now replace AND gate with input bubble with the NOR gate. Now we have circuit which is fully implemented with just NOR gates.



Realization of logic gates using NOR gates

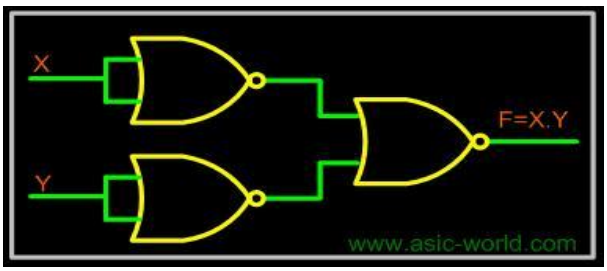
Implementing an inverter using NOR gate

Input	Output	Rule
(X+X)'	= X'	Idempotent



Implementing AND using NOR gates

Input	Output	Rule
((X+X)'+(Y+Y)')'	=(X'+Y')'	Idempotent
	= X".Y"	DeMorgan
	= (X.Y)	Involution

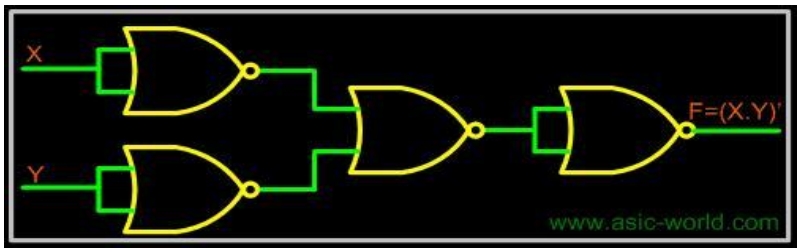


Implementing OR using NOR gates

Input	Output	Rule
((X+Y)'+(X+Y)')'	= ((X+Y)')'	Idempotent

Implementing NAND using NOR gates

Input	Output	Rule
((X+Y)'+(X+Y)')'	= ((X+Y)')'	Idempotent
	= X+Y	Involution
	= (X+Y)'	Idempotent



Arithmetic circuits are the ones which perform arithmetic operations like addition, subtraction, multiplication, division, parity calculation. Most of the time, designing these circuits is the same as designing muxers, encoders and decoders.

In the next few pages we will see few of these circuits in detail.

Adders

Adders are the basic building blocks of all arithmetic circuits; adders add two binary numbers and give out sum and carry as output. Basically we have two types of adders

- Half Adder.
- Full Adder.

Half Adder

Adding two single-bit binary values X, Y produces a sum S bit and a carry out C-out bit. This operation is called half addition and the circuit to realize it is called a half adder

Truth Table

X	Y	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Symbol

S (X,Y) = ∑(1,2)

S = X'Y + XY'

S = X⊕Y

CARRY(X,Y) = ∑(3)

CARRY = XY

Circuit

Full Adder

Full adder takes a three-bits input. Adding two single-bit binary values X, Y with a carry input bit C-in produces a sum bit S and a carry out C-out bit.

Truth Table

X	Y	Z	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

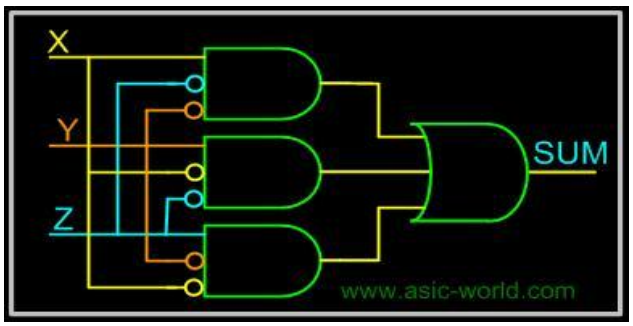
SUM (X,Y,Z) = (1,2,4,7)

CARRY (X,Y,Z) = (3,5,6,7)

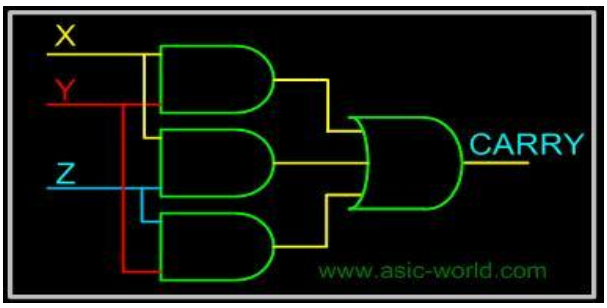
Full Adder using AND-OR

The below implementation shows implementing the full adder with AND-OR gates, instead of using XOR gates. The basis of the circuit below is from the above Kmap.

Circuit-SUM

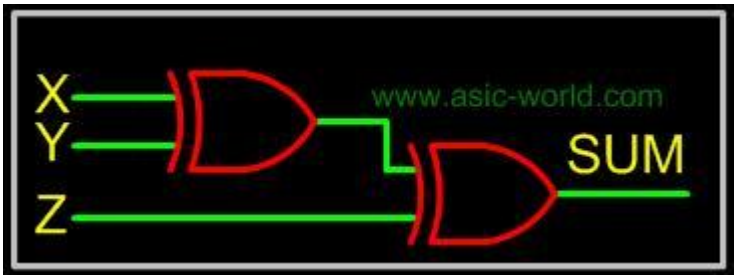


Circuit-CARRY

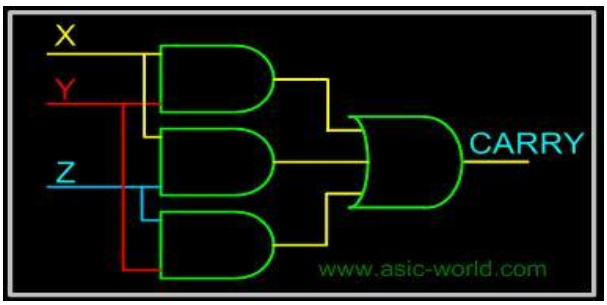


Full Adder using AND-OR

Circuit-SUM



Circuit-CARRY

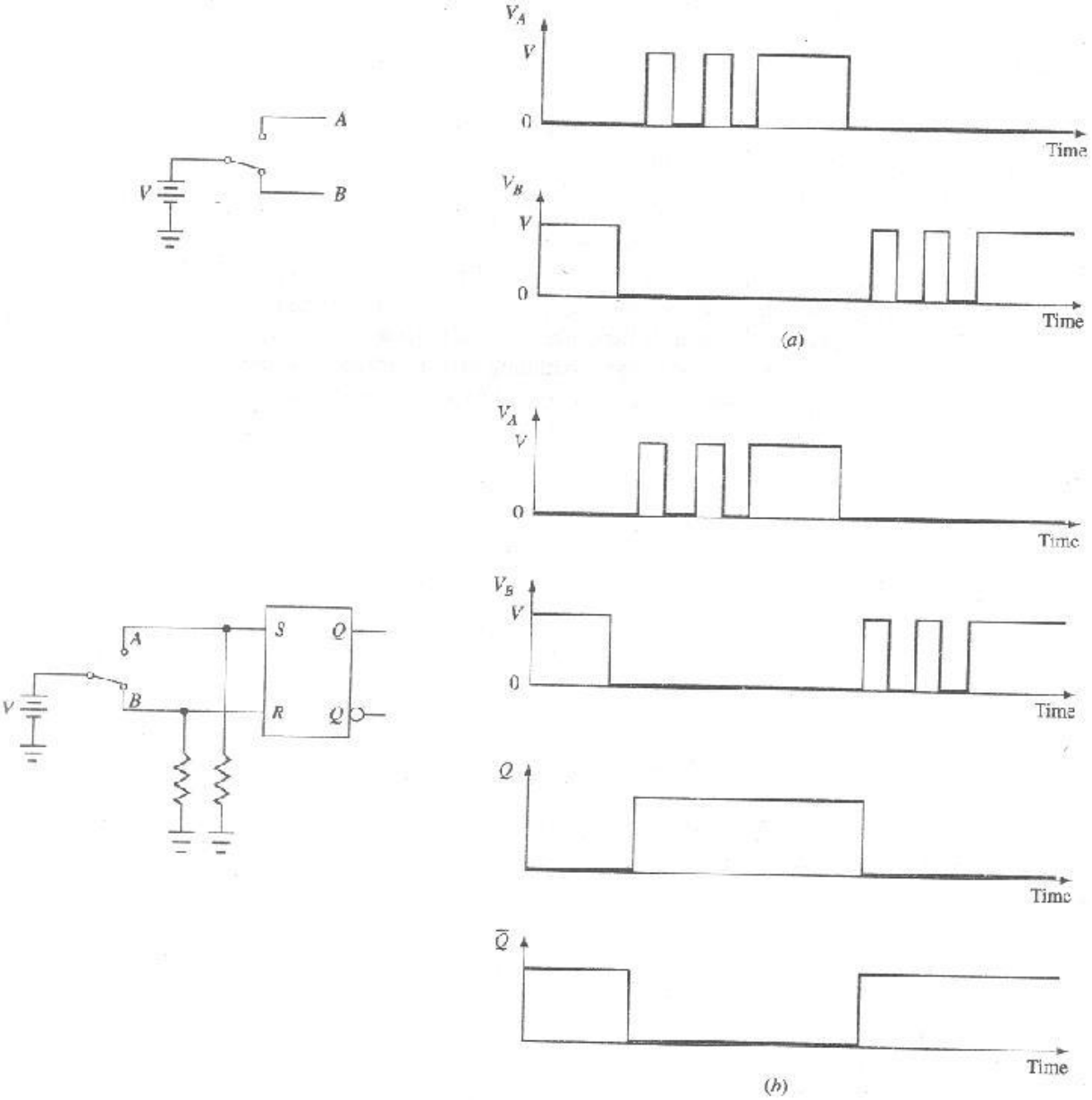


MODULE-4

FLIP FLOP

Basic Bistable element.

- Flip-Flop is Bistable element.
- It consist of two cross coupled NOT Gates.
- It has two stable states.
- Q and $\overline{Q}$ are two outputs complement of each other.
- The data stored 1 or 0 in basic bistable element is state of flip-flop.
- 1 – State is set condition for flip-flop.
- 0 – State is reset / clear for flip-flop.
- It stores 1 or 0 state as long power is ON.



Latches :

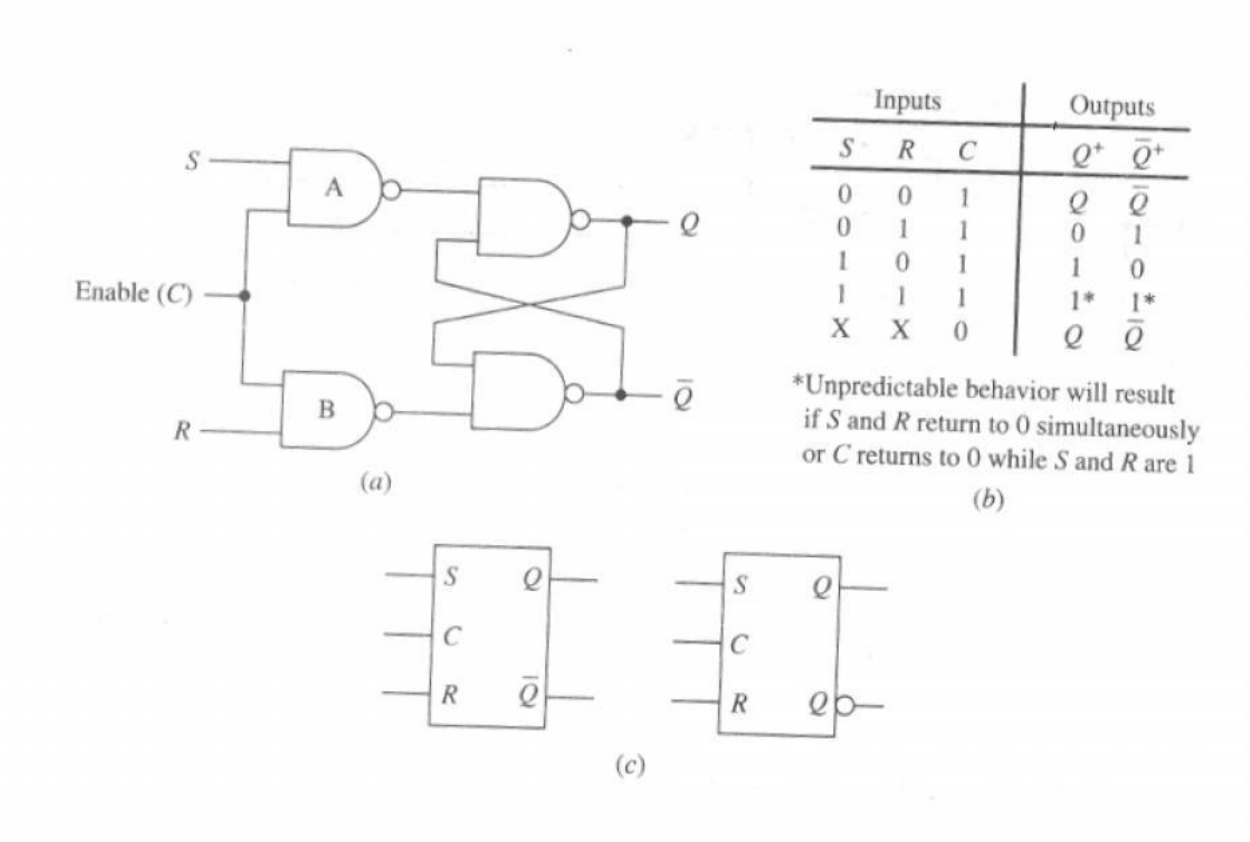
S-R Latch : Set-reset Flip-Flop

- Latch is a storage device by using Flip-Flop.
- Latch can be controlled by direct inputs.
- Latch outputs can be controlled by clock or enable input.
- Q and $\overline{Q}$ are present state for output.
- Q_+ and $\overline{Q}_+$ are next states for output.
- The function table / Truth table gives relation between inputs and outputs.
- The S=R=1 condition is not allowed in SR FF as output is unpredictable.

Application of SR Latch :

- A switch debouncer
- Bouncing problem with Push button switch.
- Debouncing action.
- SR Flip-Flop as switch debouncer.

Gated SR Latch :



- Enable input C is clock input.
- C=1, Output changes as per input condition.
- C=0, No change of state.
- S=1, R=0 is set condition for Flip-flop.

- S=0, R=1 is reset condition for Flip-flop.
- S=R=1 is ambiguous state, not allowed.

Microcontroller: A Microcontroller is a programmable digital processor with necessary peripherals. Both microcontrollers and microprocessors are complex sequential digital circuits meant to carry out job according to the program / instructions. Sometimes analog input/output interface makes a part of microcontroller circuit as mixed mode(both analog and digital) in nature.

A microcontroller can be compared to a Swiss knife with multiple functions incorporated in the same Integrated Circuits. Block diagram of a typical Microcontroller which is a true computer on a chip is shown below. The design incorporates all the features found in microprocessor CPU : ALU,PC, SP and registers. It also has other features needed to make a complete computer: ROM, RAM, Parallel I/O, serial I/O, Counters and clock circuits. Like the microprocessor , a microcontroller is a general purpose device, but one that is meant to read data, perform limited calculations on that data and control its environment based on those calculations. The prime use of microcontroller is to control the operation of a machine using a fixed program that is stored in ROM and that does not change over the lifetime of the system.

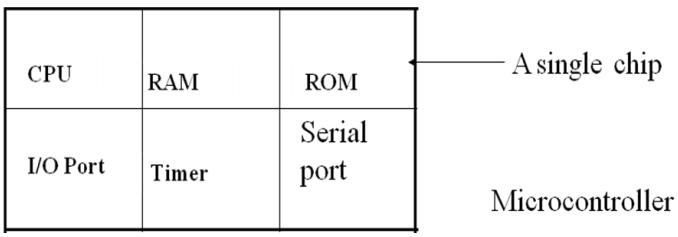


Fig3. Block diagram of a single chip computer

Complex Instruction Set Computer (CISC):

Memory in those days was expensive. Bigger programs required more storage which included more money . There was a need to reduce the number of instructions per program . This was achieved by having multiple operations within single instruction. Multiple operations lead to many different kinds of instructions .Access to memory in turn makes the instruction length variable and fetch-decode execute time unpredictable – making it more complex. Thus hardware was made to understand the complexity of instruction set. The computer having such instruction set was named as Complex Instruction Set Computer (CISC). Intel 8051 is an example for CISC architecture.

Reduced Instruction Set Computer (RISC):

In applications which require more of input , output related operations having few simple instructions that are of the same length allows memory access only with explicit load and store instructions. Hence each instruction performs less work but instruction execution time among different instructions is consistent. This would lead to instruction execution by hardware including multiple number of registers inside CPU. The computer using such instructions is called Reduced Instruction Set Computer (RISC). PIC microcontroller manufactured by Microchip Company is an example for RISC architecture.

Von neumann (Princeton) and Harvard Architecture :

Intel's 8051 employs Harvard architecture. A microcontroller has some embedded peripherals and Input/Output (I/O) devices. The data transfer to these devices takes place through I/O registers.

In a microprocessor, input /output (I/O) devices are externally interfaced and are mapped either to memory address (memory mapped I/O) or a separate I/O address space (I/O mapped I/O). There are two possible architectures one is Princeton (Von Neumann) and another is Harvard .I/O Registers space in Princeton architecture have only one memory interface for program memory (ROM) and data memory (RAM). One option is to map the I/O Register as a part of data memory or variable RAM area (memory mapped I/O). Alternatively a separate I/O register space can be assigned (I/O Mapped I/O) . Both the arrangements are shown in Fig.4.

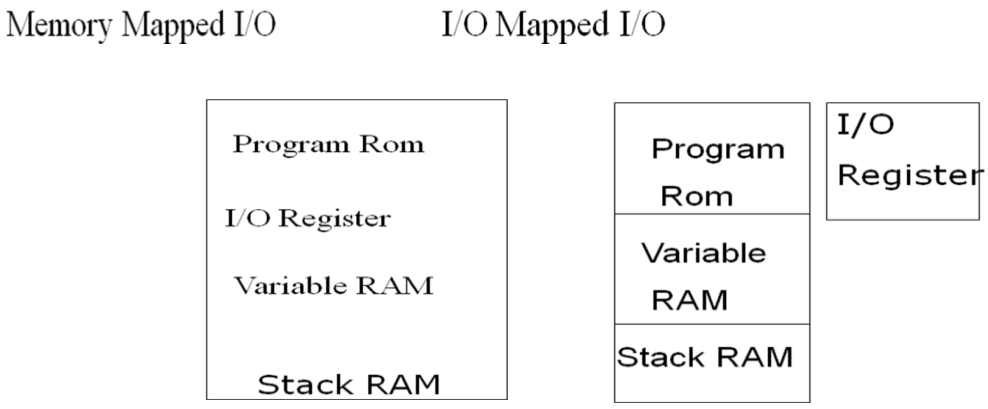


Fig 4. Input/Output Registers in Princeton Architecture

As shown in Fig 4. Program memory and Data memory are together in both the arrangements. The Princeton or Von neumann architecture one bus is used to carry the address and data with an appropriate multiplexing technique ,which in turn reduces the cost. But Harvard architecture which 8051 employs has separate Data memory and separate Code or Program memory . The Fig. 5 and Fig .6 show the need for separate address and data bus for each Program and Data memory in Harvard architecture. Since there are separate bus for access the operation of fetching the code and data can happen simultaneously which increases the speed of operation of execution inside CPU.

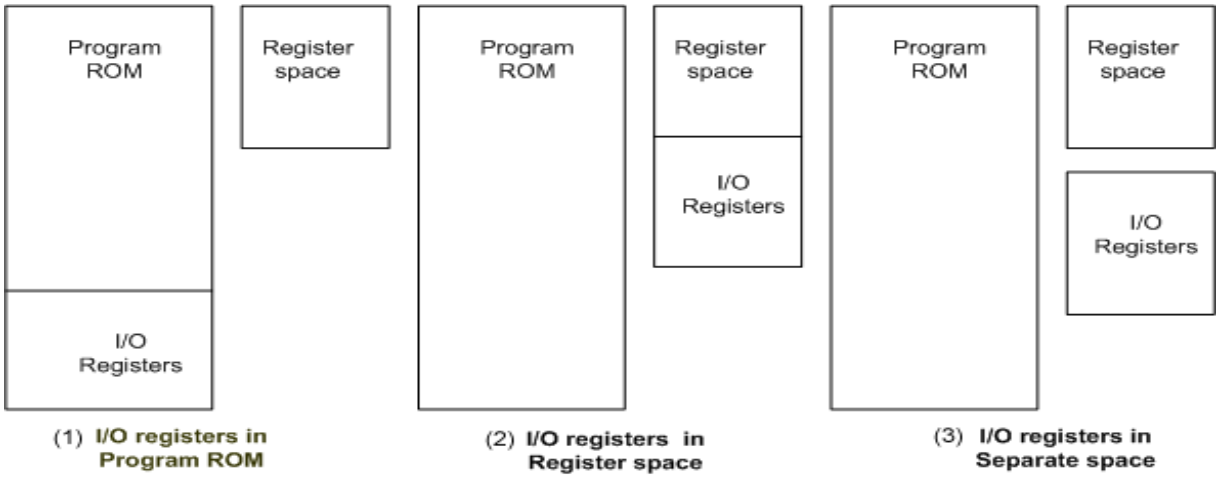


Fig. 5.Organization of I/O registers in Harvard Architecture

In Fig. 5 , the first option is difficult to implement as there is no means to write to program ROM area. It is also complicated to have a separate I/O space as shown in (3). Hence the second option where I/O registers are placed in the register space is widely used in Harvard architecture.

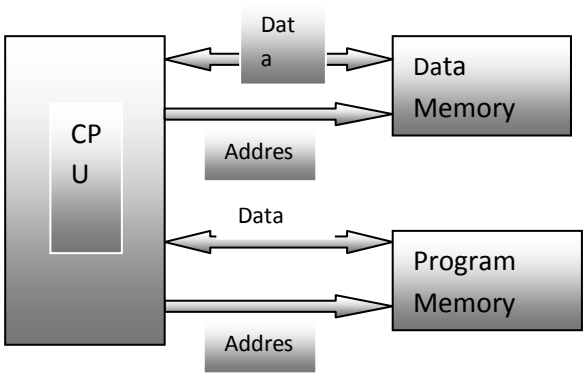


Fig6. Harvard Architecture

Computer Software: A set of instructions written in a specific sequence for computer to solve a specific task is called a program, and software is collection of programs. The program stored in the computer memory in the form of 0s and 1sand it is called as machine level instructions. Since it would be difficult to remember machine codes in the form of binary numbers an intermediate level of language for programming, between higher and machine level was developed and is known as assembly level language . Assembly language programs are written using assembly instructions known as mnemonics.

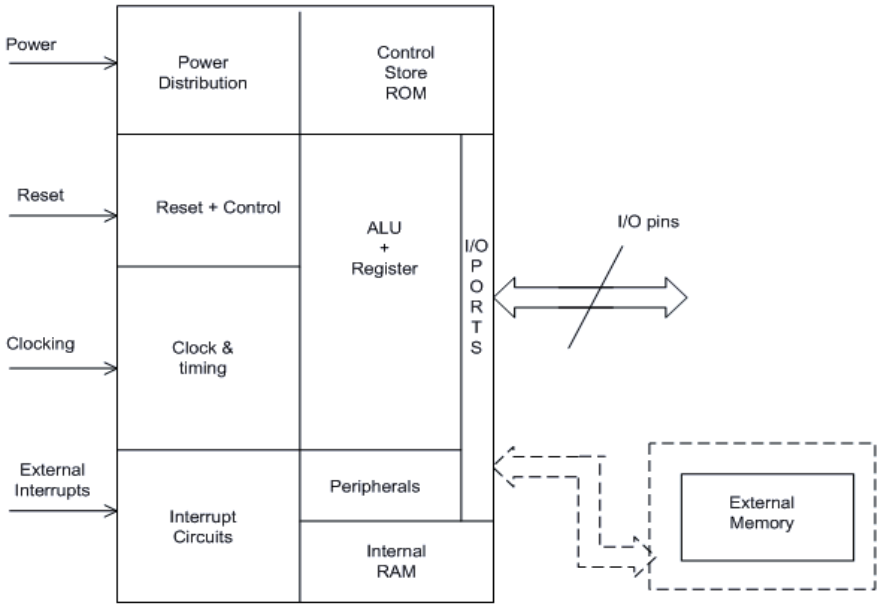
For example in CLR A, instruction CLR means clear and A means accumulator. The program mnemonics are converted to machine codes in the form of binary by a software called *Assembler*.

The Assembly language programming requires a detailed knowledge of the architecture with which the program is executed. In order to overcome the drawback of assembly language programming Higher level language like C,C++ are introduced where an interpreter or a compiler takes care of translating a higher level source code into machine codes.

Development/Classification of microcontrollers : Microcontrollers have gone through a silent evolution (invisible). The evolution can be rightly termed as silent as the impact or application of a microcontroller is not well known to a common user, although microcontroller technology has undergone significant change since early 1970's. Development of some popular microcontrollers is given as follows.

Intel 4004	4 bit (2300 PMOS trans, 108 kHz)	1971
Intel 8048	8 bit	1976
Intel 8031	8 bit (ROM-less)	.
Intel 8051	8 bit (Mask ROM)	1980
Microchip PIC16C64	8 bit	1985
Motorola 68HC11	8 bit (on chip ADC)	.
Intel 80C196	16 bit	1982
Atmel AT89C51	8 bit (Flash memory)	.
Microchip PIC 16F877	8 bit (Flash memory + ADC)	.

We use more number of microcontrollers compared to microprocessors. Microprocessors are primarily used for computational purpose, whereas microcontrollers find wide application in devices needing real time processing and control. Application of microcontrollers are numerous. Starting from domestic applications such as in washing machines, TVs, air conditioners, microcontrollers are used in automobiles, process control industries , cell phones, electrical drives, robotics and in space applications.


Power
Power Distribution
Control Store ROM
Reset
Reset + Control
ALU + Register
I/O PORTS
I/O pins
Clocking
Clock & timing
External Interrupts
Interrupt Circuits
Peripherals
Internal RAM
External Memory

MODULE-5

COMMUNICATION SYSTEMS

Radio Broadcasting, Transmission and Reception

Radio communication means the radiation of radio waves by the transmitting station, the propagation of these waves through space and their reception by the radio receiver.

Fig.7.1 below shows the general principle of radio broadcasting, transmission and reception. It essentially consists of transmitter, transmission of radio waves and radio receiver.

Transmitter-

It essentially consists of microphone, audio amplifiers, oscillator and modulator.

A microphone is a device which converts sound waves into electrical waves. The output of microphone is fed to multistage audio amplifier for raising the strength of weak signal.The job of amplification is performed by cascaded audio amplifiers. The amplified output from the last audio amplifier is fed to the modulator for rendering the process of modulation.The function of the oscillation is to produce a high frequency signal called a carrier wave. Usually crystal oscillator is used for the purpose.The amplified audio signal and carrier waves are fed to the modulator. Here the audio signal is superimposed on the carrier wave in suitable manner. The resultant waves are called modulated waves, and the process is called modulation. The process of modulation permits the transmission of audio signal at the carrier signal (frequency). As the carrier frequency is very high, therefore the audio signal can be transmitted to large distances. The radio waves from the transmitter are fed to the transmitting antenna or aerial from where these are radiated into space.

The transmitting antenna radiates the radio waves in space in all directions. These radio waves travel with the velocity of light $3x10^8$ m/sec. The radio waves are electromagnetic waves and possess the same general properties.

Receiver-

On reaching the receiving antenna, the radio waves induce tiny emf in it. This small voltage is fed to the radio receiver. Here the radio waves are first amplified and then signal is extracted from them by the process of demodulation. The signal is amplified by audio amplifiers and then fed to the speaker for reproduction into sound waves.

Need for modulation

The advantages of using modulation technique is given below :

- Reduce the height of the antenna
- Increase the range of communication

- Avoids mixing of signals
- Allows multiplexing of signals
- Improves the signal to noise ratio.
- Avoids interference of the bands by providing gaurd band
- Improve quality of reception
- Provide possibility for wireless transmission.

1. **Practical Antenna length-**theory shows that in order to transmit a wave effectively the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$wavelength = \frac{Velocity}{frequency} = \frac{3 \times 10^8}{frequency\ (Hz)}\ metres$$

As the audio frequencies range from 20 Hz to 20Khz, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For example to radiate a frequency of 20 KHz directly into space we would need an antenna length of $3x10^8$ /$20x10^3$ ≈ 15,000 meters. This is too long to be constructed practically. But instead we operate at higher frequencies, say in MHz range, the antenna dimension comes down.The operation at this frequencies is possible only with modulation techniques.

2. **Operating Range-** The energy of a wave depends upon its frequency. The greater the frequency of the wave, the greater the energy possessed by it. As the audio signal frequencies are small, therefore these cannot be transmitted over large distances if radiated directly into space.
3. **Avoids mixing of signals :** The transmission band of 20Hz to 20KHz contains many signals generated from different sources. These signals are translated to different portion of the electromagnetic spectrum called channels, having different band widths, by providing different carrier frequencies.These frequencies are separated at the receiver while receiving.
4. Allows multiplexing of signals**;** The modulation permits multiplexing of signals, meaning simultaneous transmission of more signals on the same channel.Example MW and SW transmission with frequencies allotted to different bands and transmitted on the same channel
5. **Improves the signal to noise ratio.:** The baes band signals which are in the audio frequency range are susceptible to noise. The radio frequencies which are used for modulation are immune to noise. Hence modulating the message signals with the carrier helps in improving the signal to noise ratio.
6. **Avoids interference of the bands by providing gaurd band** : Special guard bandsare provided between bands to guard the interference of adjacent band signals.This is usually around 25KHz.
7. **Improve quality of reception :** Different techniques of transmission like digital modulation improves the quality of reception by reducing the noise in the system.
8. **Wireless communication-** Radio transmission should be carried out without wires.

Modulation- The process of changing some characteristics (example amplitude, frequency or phase) of a carrier wave in accordance with the intensity of the signal is known as modulation.

Types of modulation-

1. Amplitude modulation
2. Frequency modulation
3. Phase modulation

1. Amplitude modulation

When the amplitude of high frequency carrier wave is changed in accordance with the intensity of the signal, it is called amplitude modulation.

The following points are to be noted in amplitude modulation .

1. The amplitude of the carrier wave changes according to the intensity of the signal.
2. The amplitude variations of the carrier wave is at the signal frequency f_S.
3. The frequency of the amplitude modulated wave remains the same ie.carrier frequency f_C. es

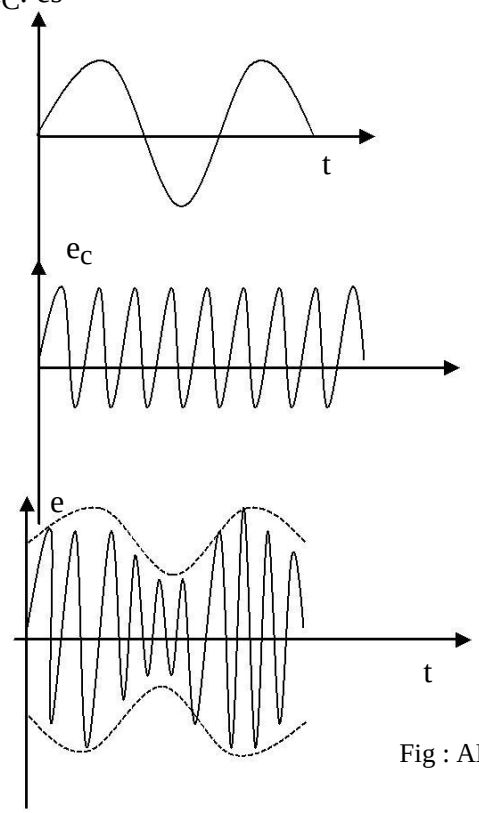
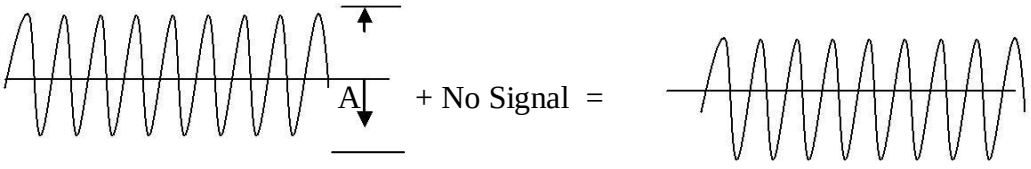


Fig : AM waveforms

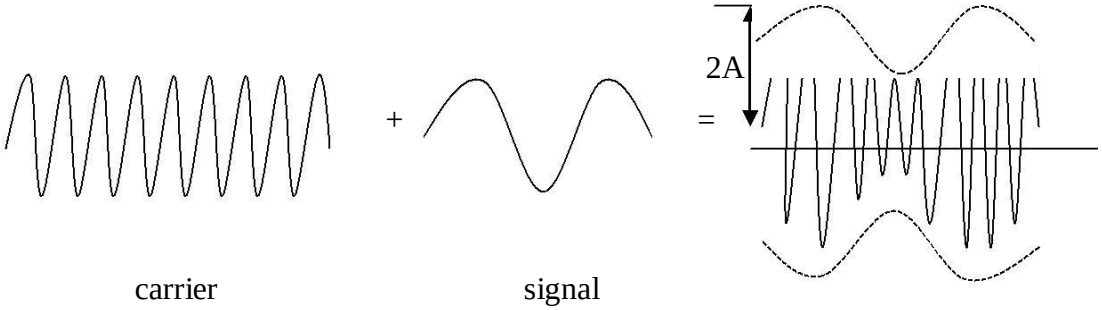
Modulation factor

The ratio of change of amplitude of carrier wave to the amplitude of normal carrier wave is called modulation factor.

m=(amplitude change of carrier wave) / normal carrier wave(unchanged)



carrier m=0/A = 0%

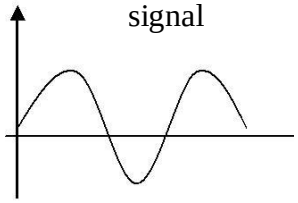


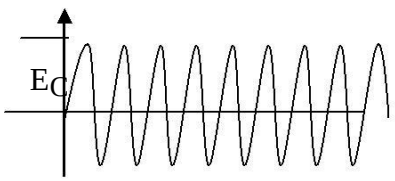
carrier signal

m=(2A-A)/A =1

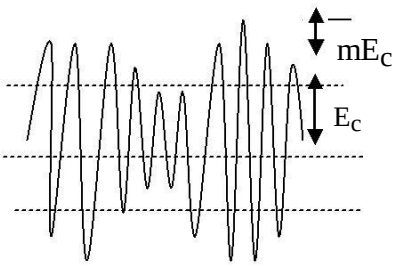
Modulation factor is very important since it determines the strength and quality of the transmitted signal. The greater the degree of modulation, the stronger and clearer will be the audio signal. It should be noted that if the carrier is overmodulated (ie m>1) distortion will occur at reception.

Analysis of amplitude modulated wave





Carrier



AM Wave

- A carrier wave is represented by $e_c = E_c \cos w_c t$----------(1)

  Where e_c ------instantaneous voltage of carrier.

  E_c ----- amplitude of carrier.

- In amplitude modulation, the amplitude E_C of the carrier wave is varied in accordance with intensity of the signal as shown in figure.
- Suppose m=modulation index, then change in carrier amplitude $=mE_c$. Amplitude or E_{max} of the signal = mE_c.

  $e_s = mE_c \cos w_s t$----------(2)

  where mE_c is the amplitude of the signal.

  e_s ---------instantaneous voltage of the signal.

The amplitude of the carrier varies at signal frequency fs. Therefore the amplitude of AM wave is given by,

$$E_c + mE_c \cos w_s t = E_c(1 + m \cos w_s t)$$

- The instantaneous voltage of AM wave is,

  e = Amplitude x $\cos w_c t$

$$e = E_C (1 + m \cos w_s t) \cos w_c t$$

$$= E_C \cos w_c t + mE_C \cos w_s t \cos w_c t$$

$$= E_C \cos w_c t + \frac{mE_C}{2}[2 \cos w_s t \cos w_c t]$$

$$= E_C \cos w_c t + \frac{mE_c}{2}[\cos(w_c + w_s)t + \cos(w_c - w_s)t]$$

$$\therefore e = E_C \cos w_c t + \frac{mE_c}{2}\cos(w_c + w_s)t + \frac{mE_c}{2}\cos(w_{cs} - w)t \text{ - - - - - - - - - - - - (3)}$$

- The AM wave is equivalent ot thesummatoin of theree sinusoidal waves: aone having amplitude E_C and frequency f_c, the second having amplitde $mE_c/2$ and frequency $(f_c + f_s)$ and the third having amplitude $mE_c/2$ and frequency $f_c - f_s$..
- The AM wave consists three frequencies viz, f_c, f_c+f_s . The first frequency is the carrier frequency. Thus the process of modulation doesnot change the original carrier frequency but produces two new frequencies f_c+f_s and $f_c - f_s$. which are called sideband frequencies.
- In amplitude modulation the bandwidth is from $f_c - f_s$. to f_c+f_s ie $2f_s$ ie twice the signal frequency.
- Frequency spectrum of an amplitude modulated wave is shown in figure below

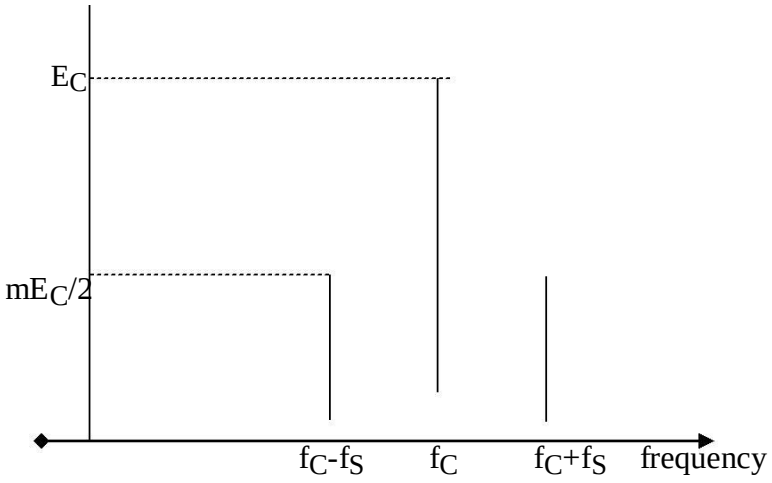


Fig7.3: Frequency Spectrum of AM wave

from equation (3),

$$\text{carrier power } P_C = \frac{\left(\frac{E_c}{\sqrt{2}}\right)^2}{R} = \frac{E_C^2}{2R} \text{ ----------(4)}$$

$$\text{Total power of sidebands } P_S = \frac{\left(\frac{mE_C}{\sqrt{2}}\right)^2}{R} + \frac{\left(\frac{mE_C}{2\sqrt{2}}\right)^2}{R} = \frac{m^2 E_C^2}{4R} \text{ -------(5)}$$

$$\text{Total power of AM wave } P_T = P_C + P_S$$

$$= \frac{E_c^2}{2R} + \frac{m^2 E_c^2}{4R} = \frac{E_c^2}{2R}\left[1 + \frac{m^2}{2}\right]$$

$$= \frac{E_C^2}{2R}\left[\frac{2+m^2}{2}\right] \text{ ----------(6)}$$

Also fraction of total power carried by sidebands,

$$\frac{P_s}{P_T} = \frac{equn\ (5)}{equn\ (6)} = \frac{m^2}{2+m^2} \text{ ----------(7)}$$

Demodulation

The process of recovering the audio signal from the modulated wave is known as demodulation or detection.

At the broadcasting station, modulation is done to transmit the audio signal over larger distances. When the modulated wave is picked up the receiver, it is necessary to recover the audio signal from it. This process is accomplished in the radio receiver and is called demodulation.

Envelope Detector

The envelope of a signal is its maximum value over a set sampling period. A diode circuit used most often to detect the envelope of AM signals is the simplest and the universal method of demodulating AM signals. The prerequisite for the use of this demodulation method is the presence of a strong carrier and high SNR. Excessive amount of noise causes severe envelope fluctuations and makes this method less effective. We all know of the AM radio's vulnerability to noise and other atmospheric perturbations.

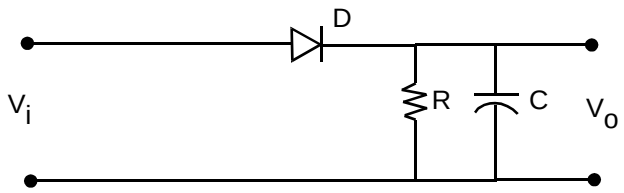


Figure : RC-Diode Circuit used for Envelope Demodulation

The envelope detector is basically a Diode-RC circuit as shown above. The signal is applied to the terminals of the circuit. The Diode conducts as the voltage(amplitude) increases and the capacitor charges up. Now as the voltage begins to go down, resistor discharges and the capacitor lets go of its charge. The cycle continues and each charge of the capacitor indicates the maximum value over that period. In fact the capacitor discharges slightly between cycles as shown in the figure below but this can be compensated for easily.

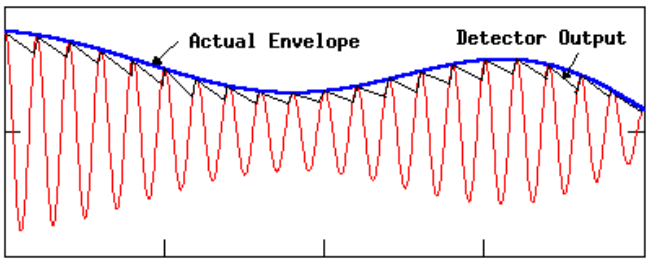


Figure :Envelope Detection up-close

Limitations of Amplitude Modulation

1. **Noisy Reception-** In an AM wave, the signal is in the amplitude variations of the carrier. Practically all the natural and man made noises consist of electrical amplitude disturbances. As a radio receiver cannot distinguish between amplitude variations that represent noise and those that contain the desired signal. Therefore reception is very noisy.

2. **Low efficiency-** In AM useful power is in the sidebands as they contain the signal. An AM wave has low sideband power.

   For example even if modulation is 100 % ie m=1.

$$\frac{P_s}{p_T} = \frac{m^2}{2+m^2} = \frac{1}{2+1} = 0.33$$

$$P_S = 33\% \text{ of } P_T$$

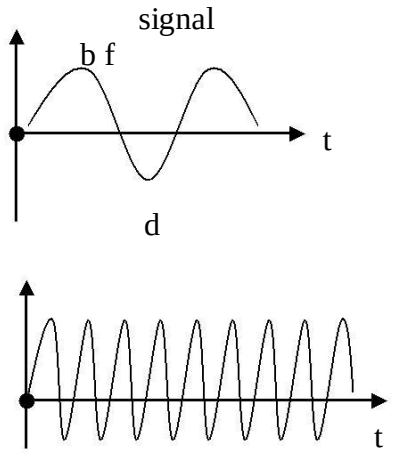
Sideband power is only one-third of the total power of AM wave. Hence efficiency of this type of modulation is low.

3. **Lack of audio quality-** In order to attain high fidelity reception, all audio frequencies upto 15 Khz must be reproduced. This necessitates a bandwidth of 30 KHz since both sidebands must be reproduced ($2f_s$). But AM broadcasting stations are assigned with bandwidth of only 10 KHz to minimize the interference from adjacent broadcasting stations. This means that the highest modulating frequency can be 5 Khz which is hardly sufficient to reproduce the music properly.

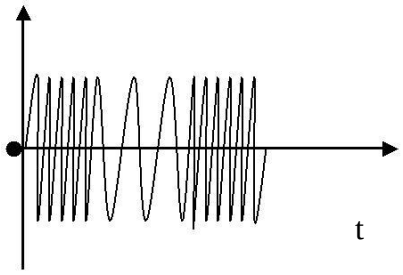
Frequency modulation

" When the frequency of carrier wave is changed in accordance with the intensity of the signal, it is called frequency modulation".

- Here the amplitude of the modulated wave remains the same ie carrier wave amplitude.
- The frequency variations of carrier wave depend upon the instantaneous amplitude of the signal.
- When the signal approaches positive peaks as the B and F, the carrier frequency is increased to maximum and during negative peak, the carrier frequency is reduced to minimum as shown by widely spaced cycles.



Carrier



Advantages of FM

1. It gives noiseless reception.
2. The operating range is quite large.
3. The efficiency of transmission is very high.

Comparision of AM and FM.

Amplitude Modulation	Frequency Modulation
1) The amplitude of the carrier is varied In accordance with the signal	The frequency of the carrier is varied in accordance with the signal
2) The modulation index 'm' is <1	The modulation index 'β' is >1
3) Transmitted power is dependent on modulation index 'm'	Transmitted power is independent on modulation index 'β'
4) The amplitude of the side bands are dependent on the modulation index'm' and are always less than the carrier	The amplitude of the side bands are vary with the modulating index and can be calculated using Bessel functions
5) Contains only two side bands	Contains multiple side bands
6) Susceptible to noise due to The method of modulation used.	Immune to noise as amplitudes are Clipped
7) Less efficient as carrier contains more power than side bands	More efficient as it contains more side bands and hence more signal power.

TRANSDUCERS

Nearly all engineering applications require some form of measuring, controlling, calculating, communicating and recording of data. These operations, grouped or isolated, are inherent in measurement instrumentation. If the equipment is to be used for the quantitative analysis of an analogue signal, i.e., a naturally occurring signal, the following must be taken into consideration

The analogue signal to be measured may be temperature, pressure, humidity, velocity, flow rate, linear motion, position, amongst others. This signal must be converted into an analogue electrical signal, typically voltage or current, and then into a digital form that can be processed by an electronic circuit. The first task (see Fig. 1) requires sensors to convert the physical quantities into electrical signals. Generally, the broad definition of a sensors/ transducers includes devices which convert physical quantities (mechanical force) into analogue electrical signal (in the range of millivolts or milliamps).

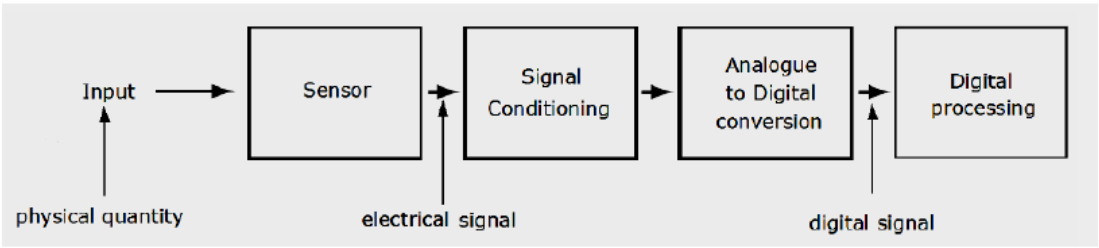


Fig. 1 Data acquisition block diagram

Classification of Transducers

The Classification of Transducers is done in many ways. Some of the criteria for the classification are based on their area of application, Method of energy conversion, nature of output signal, According to Electrical principles involved, Electrical parameter used, principle of operation, & Typical applications.

The transducers can be classified broadly

i. On the basis of transduction form used

ii. As primary and secondary transducers

iii. As active and passive transducers

iv. As transducers and inverse transducers.

Broadly one such generalization is concerned with energy considerations wherein they are classified as active & Passive transducers.

A component whose output energy is supplied entirely by its input signal (physical quantity under measurement) is commonly called a 'passive transducer'. In other words the passive transducers derive the power required for transduction from an auxiliary source. Active transducers are those which do not require an auxiliary power source to produce their output. They are also known as self generating type since they produce their own voltage or current output. Some of the passive transducers (electrical transducers), their electrical parameter (resistance, capacitance, etc), principle of operation and applications are listed below.

Self-Generating Transducers (No External Power) – Active Transducers

1. Thermocouple and thermopile

Principle of operation: An emf is generated across the junction of two dissimilar metals or semiconductors when that junction is heated.

Applications: Temperature, heat flow, radiation

2. Moving-coil generator

Principle of operation: Motion of a coil in a magnetic field generates a voltage.

Applications: Velocity. vibration

3. Piezoelectric pickup

An emf is generated when an external force is applied to certain crystalline materials,

such as quartz Sound, vibration. acceleration, pressure changes

4. Photovoltaic cell

Principle of operation: A voltage is generated in a semi-conductor junction device when

radiant energy stimulates the cell

Applications: Light meter, solar cell

Resistive Transducers

The resistance of a metal conductor is expressed by a simple equation that involves a few physical quantities. The relationship is R = _L/A, where R = resistance _, L = length of conductor m. A = cross-sectional area of conductor ; m2, and _ = resistivity of conductor material ; _m.

Any method of varying one of the quantities involved in the above relationship can be the design basis of an electrical resistive transducer.

Strain gauges

Strain gauges work on the principle that the resistance of a conductor or a semiconductor changes when strained. This property can be used for measurement of displacement, force and pressure. The resistivity of materials also changes with change of temperature thus causing a change of resistance. If a metal conductor is stretched or compressed, its resistance changes on account of the fact that both length and diameter of conductor change. Also there is a change in the value of resistivity of the conductor when it is strained and this property is piezoresistive effect. Therefore, resistance strain gauges are also known as piezoresistive gauges.

The strain gauges are used for measurement of strain and associated stress in experimental stress analysis. Secondly, many other detectors and transducers, notably the load cells, torque meters, diaphragm type pressure gauges, temperature sensors, accelerometers and flow meters, employ strain gauges as secondary transducers.

Theory of Strain Gauges

The change in the value of resistance by straining the gauge may be partly explained by the normal dimensional behaviour of elastic material. If a strip of elastic material is subjected to tension, as shown in Fig.1 or in other words positively strained, its longitudinal dimension will increase while there will be a reduction in the lateral dimension

LVDT: DISPLACEMENT TRANSDUCERS

The concept of converting an applied force into a displacement is basic to many types of transducers. The mechanical elements that are used to convert the applied force into a displacement are called *force-summing* devices.

Some of the Force-summing Devices Used by *Pressure* transducers are

1) Diaphragm, flat or corrugated
2) Bellows
3) Bourdon tube, circular or twisted
4) Straight tube

Some of the Force-summing Devices Used in *accelerometer* and *vibration* pickups are

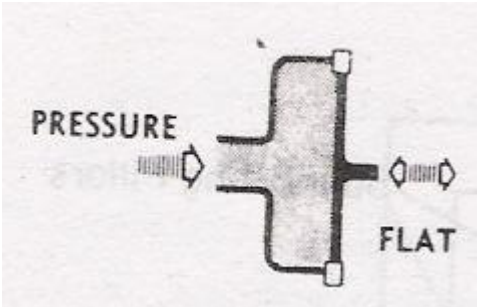
1)Mass cantilever, single or double suspension

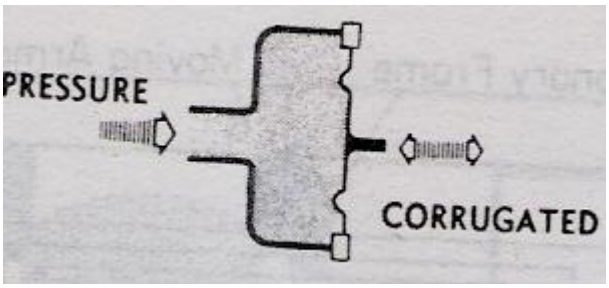
2)Pivot torque

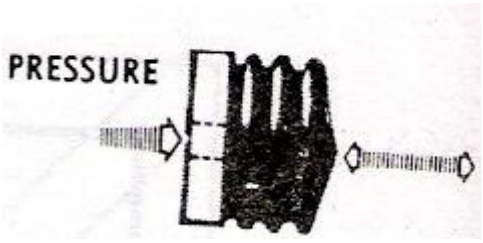
The above Force-summing Devices are shown in Fig. 8

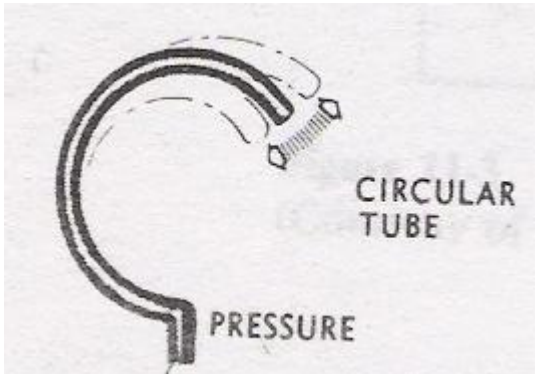
The displacement created by the action of the force-summing device is converted into a change of some *electrical* parameter.

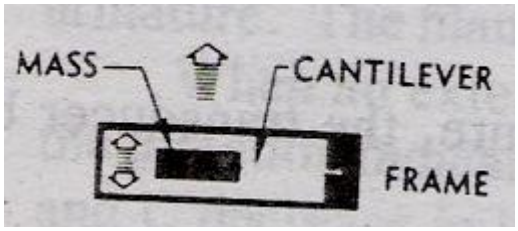
The electrical principles commonly used in the measurement of displacement are Capacitive, Inductive , Differential transformer, Ionization, Oscillation, Photoelectric, Piezoelectric, Potentiometric











Linear Variable Differential Transformer – LVDT Transducer

The differential transformer transducer measures force in terms of the displacement of the ferromagnetic core of a transformer. The basic construction of the LVDT is given in Fig, 9.

The transformer consists of a single primary winding and two secondary windings which are placed on either side of the primary. The secondaries have an equal number of turns but they are connected in series opposition so that the emfs induced in the coils OPPOSE each other. The position of the movable core determines the flux linkage between the ac-excited primary winding and each of the two secondary winding.

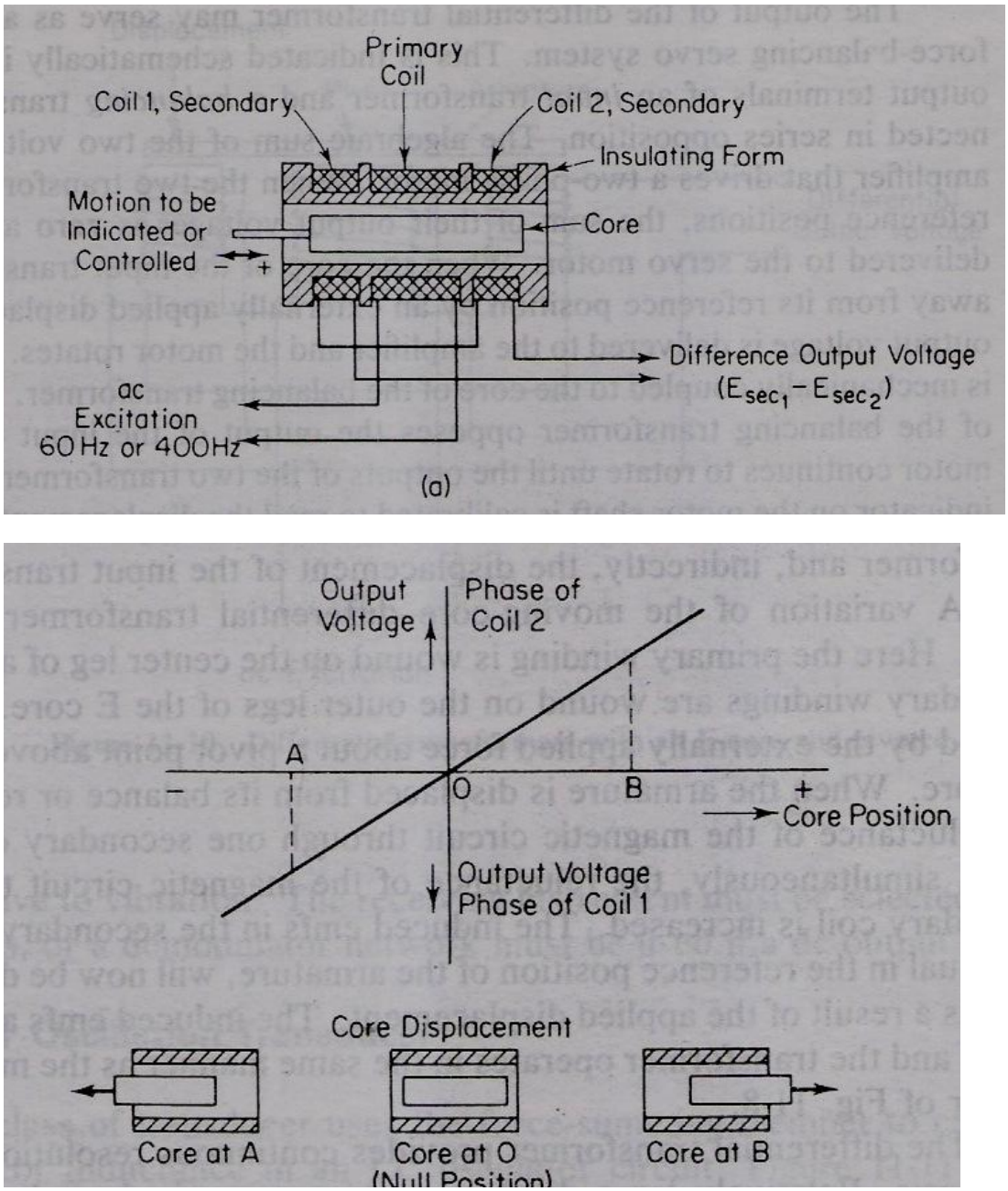


Fig. 10

Relative positions of the core generate the indicated output voltages as shown in Fig. 10. The linear characteristics impose limited core movements, which are typically up to 5 mm from the null position. With the core in the center, (or *reference* position or Fig. 11,), the induced emfs in the secondaries are equal, and since they oppose each other, the output voltage will be 0 V.

When an externally applied force moves the core to the left-hand position, more magnetic flux links the left-hand coil than the right-hand coil and the Differential Output E0 = ES1 – ES2 Is in-phase with Ei as ES1 > ES2 . The induced emf of the left hand coil is therefore larger than the

induced emf of the right-hand coil. The magnitude of the output voltage is then equal to the difference between the two secondary voltages, and it is *in phase* with the voltage of the left-hand coil.

Similarly, when the core is forced to move to the right, more flux links the right-hand coil than the left-hand coil and the resultant output voltage is now in phase with the emf of the right-hand coil, while its magnitude again equals the difference between the two induced emfs.

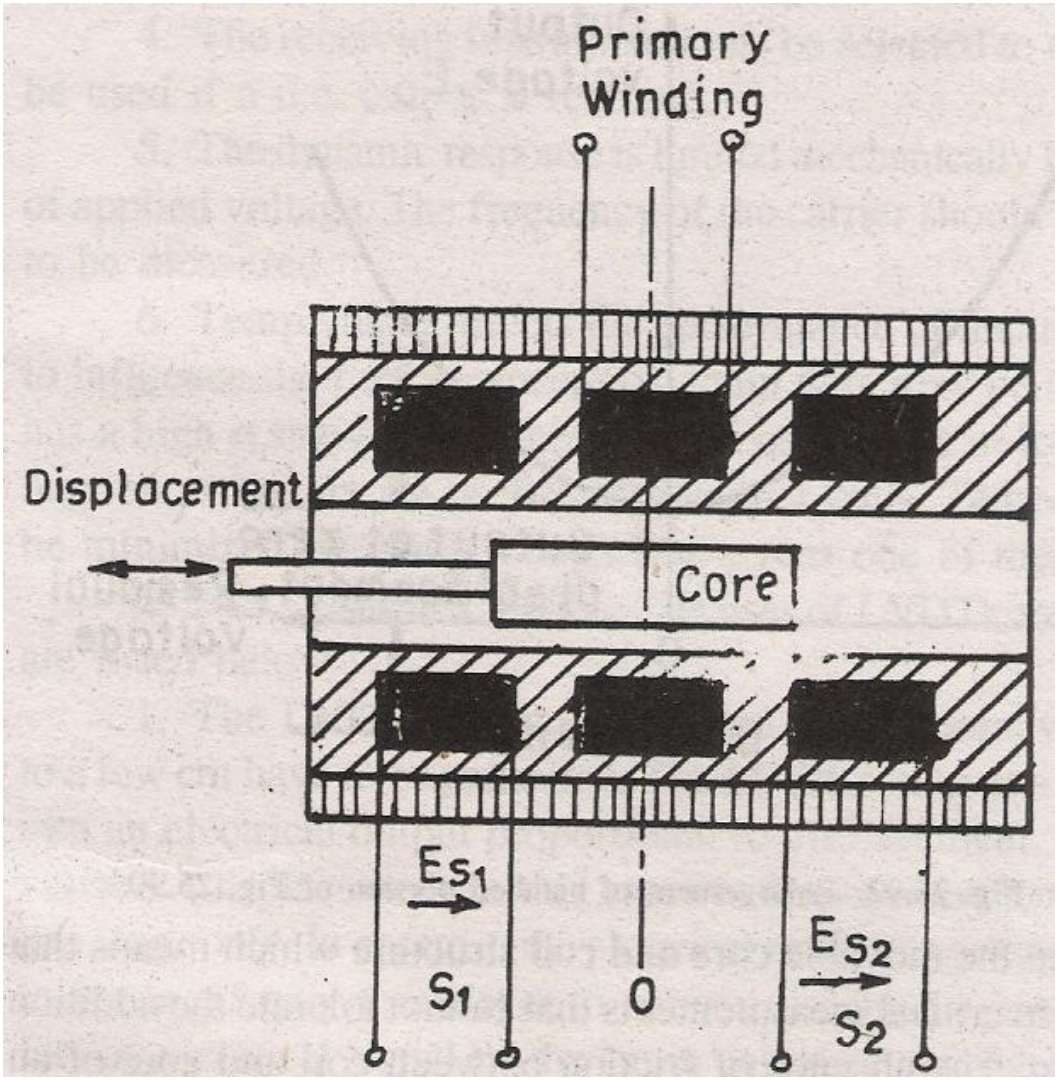
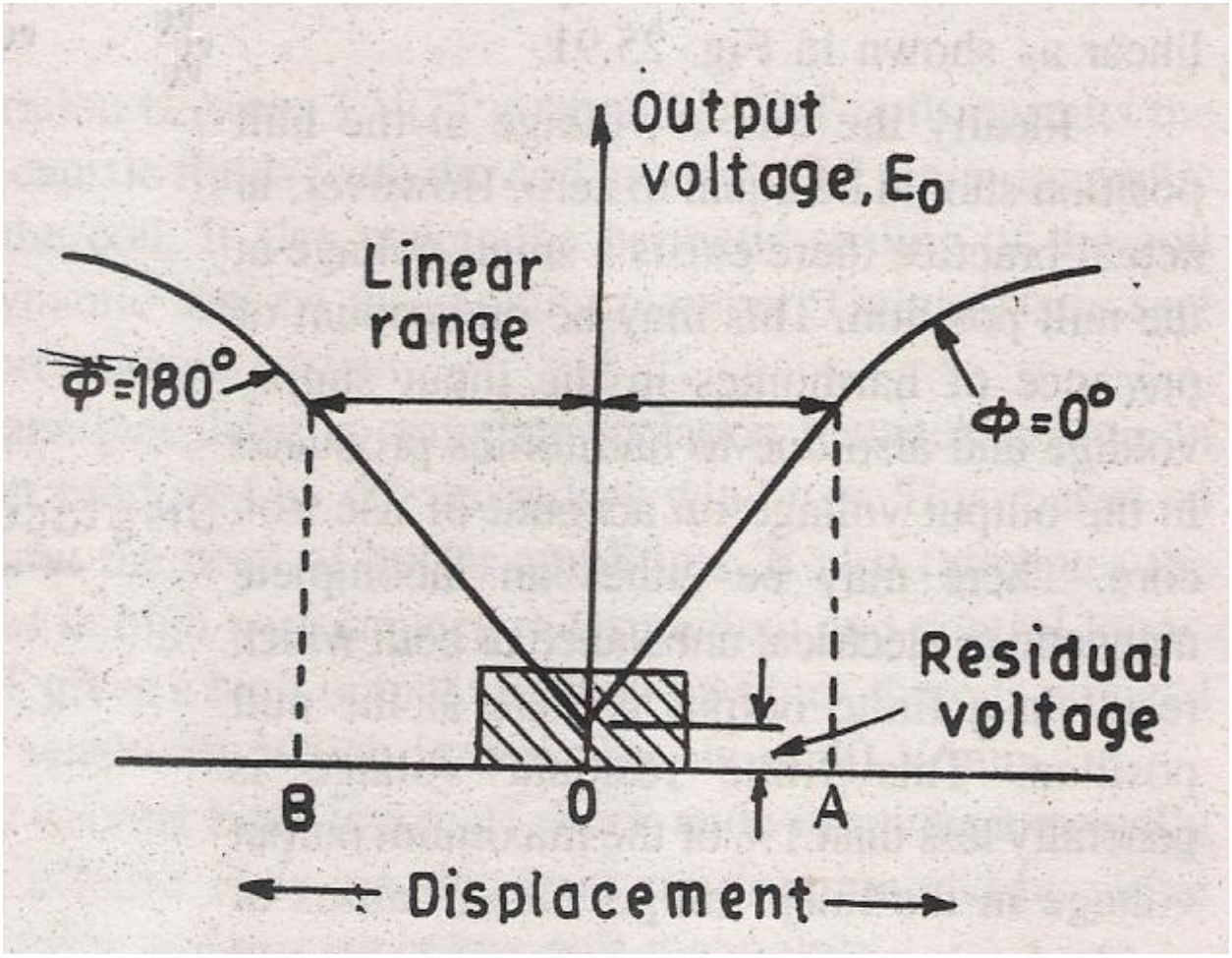


Fig.11



Ideally the output voltage at the null position should be equal to zero. In actual practice there exists a small voltage at the null position. (refer Fig. 12). This may be on account of presence of harmonics in the input supply voltage and also due to harmonics produced in the output voltage due to use of iron Displacement core. There may be either an incomplete magnetic or electrical unbalance or both which result in a finite output voltage at the null position. This finite residual voltage is generally less than 1% of the maximum output voltage in the linear range. Other causes of residual voltage are stray magnetic fields and temperature effects.

Measurement of Temperature

The principles used in the measurement of pressure are also applied in the measurement of temperature, flow and liquid levels. Hence some of the working principles of the instruments are repeated Resistance Thermometers

Resistance-temperature detectors, or resistance thermometers, employ a sensitive element of extremely pure platinum, copper, or nickel that provides definite resistance value at each temperature within its range.

Principle of working: The resistance of a conductor changes when its temperature is changed. This property is utilized for measurement of temperature. The variation of resistance R with temperature T (°K) can be represented by the following relationship for most of the metals as:

R = Ro (1 + _1T + _2T2 +.....+_nTn + ..)

where Ro = resistance at temperature *T*= 0 and _1,_2,_3,_n are constants.

The resistance thermometer uses the change in electrical resistance of conductor to determine the temperature. The resistivity of metals showing a marked dependence on temperature was discovered by Sir Humphry Davy.

RTD - resistance temperature detector

All metals produce a positive change in resistance with temperature. The requirements of a conductor material to be used in RTDs are :

(i) The change in resistance of material per unit change in temperature should be as large as possible. This implies a metal with a high value of resistivity should be used for RTDs.

ii) The material should have a high value of _ so that minimum volume of material is used Rt = Rref (1 + _ _T) A high value of _ is desirable in a temperature-sensing element so that a substantial change in resistance occurs for a relatively small change in temperature.

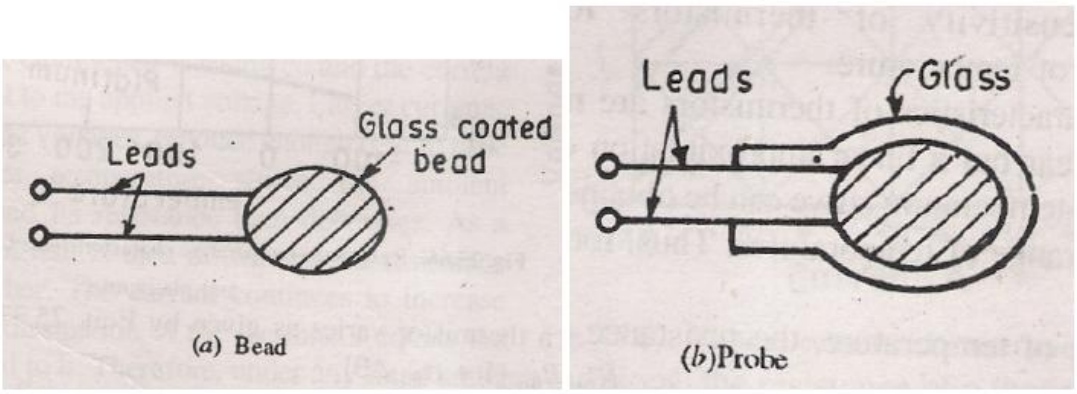
This change in resistance (_R) can be measured with a Wheatstone bridge which may be calibrated to indicate the temperature that caused the resistance change rather than the resistance itself.

Thermistors

Some materials, such as carbon and germanium, have a negative temperature coefficient of resistance that implies that the resistance decreases with an increase in temperature. Thermistors or *thermal resistors,* are semiconductor devices that behave as resistors with a high, usually *negative* temperature coefficient of resistance.

In some cases, the resistance of a thermistor at room temperature may decrease as much as 6 per cent for each 1oC rise in temperature. This high sensitivity to temperature change makes the thermistor extremely well suited to precision temperature *measurement, control.* And *compensation.* Thermistors are widely used in applications, especially in the lower temperature

range of -100'C to 300 oC. Thermistors are composed of a sintered mixture of metallic oxides, such as manganese, nickel, cobalt, copper, iron, and uranium. Their resistances range from 0.5 _ to 75 M_ and they are available in a wide variety of shapes and sizes. Smallest in size are the beads with a diameter of 0.15 mm to 1.25 mm.



Beads may be sealed in the tips of solid glass rods to form probes that are somewhat easier to mount than beads. Disks and washers are made by pressing thermistor material under high pressure into flat cylindrical shapes with diameters from 2.5 mm to 25 mm. Washers can be stacked and placed in series or in parallel for increased power dissipation.