Advanced Computer Architecture VTU CBCS Question Paper Set 2018

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10CS74

Seventh Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. List and explain four important technologies which have led to the improvements in computer system. **(10 Marks)**

b. Give a brief explanation about trends in power in integrated circuits and cost. **(10 Marks)**

2 a. With a neat diagram, explain the classic five stage pipeline for a RISC processor. **(10 Marks)**

b. What are the major hurdles of pipelining? Illustrate the branch hazards, in detail. **(10 Marks)**

3 a. Mention the techniques used to reduce branch costs. Explain static and dynamic branch prediction used for same. **(08 Marks)**

b. What are data dependencies? Mention the different types of data dependencies. Explain name dependences, with example. **(06 Marks)**

c. What is correlating predictors? Explain with example. **(06 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(08 Marks)**

b. What are the key issues in implementing advanced speculation techniques? Explain in detail. **(08 Marks)**

c. Write a note on value predictors. **(04 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(08 Marks)**

b. With a neat diagram, explain the basic structure of a centralized shared memory and distributed shared memory multiprocessor. **(06 Marks)**

c. Explain snooping with respect to cache – coherence protocol. **(06 Marks)**

6 a. Assume we have a computer where CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 cycles and miss rate is 2% how much faster would be computer if all instructions were cache hits? **(08 Marks)**

b. Briefly explain four basic cache optimization methods. **(12 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. **(10 Marks)**

b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. **(10 Marks)**

8 a. Explain detecting and enhancing loop level parallelism for VLIW. **(06 Marks)**

b. Explain intel – IA – 64 architecture, with a neat diagram. **(06 Marks)**

c. Explain hardware support for exposing parallelism for VLIW and EPIC. **(08 Marks)**

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