Microelectronic Circuits VTU CBCS Question Paper Set 2018

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10EC63

Sixth Semester B.E. Degree Examination, June/July 2013
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least THREE from Part A and TWO from Part B.***

PART – A

1 a. Derive the equation for finite output resistance of a MOSFET. **(08 Marks)**

b. For the CS-amplifier shown in Fig.Q.1(b), find R_{in}, Av_o, R_{out} and Gv with r_o taken into account. If V_{sig} is a 0.4V (P-P) what output signal results? Assume R_{sig} = 10KΩ, R_L = 15KΩ, g_m = 1 mA/v and r_o = 150KΩ. **(08 Marks)**

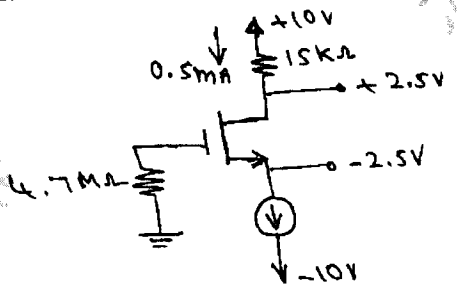

Fig.Q.1(b)

c. What is threshold voltage and mention its range? **(04 Marks)**

2 a. Draw the development of the T-equivalent circuit model for the MOSFET. **(05 Marks)**

b. Derive the voltage gain and overall voltage equations of a source follower using MOSFET. **(08 Marks)**

c. Design the circuit shown in Fig.Q.2(c) so that the transistor operates at I_D = 0.4 mA and V_D = 0.5V. The NMOS transistor has V_t = 0.7V, $\mu_n C_{ox}$ = 100 μ A/V^2, L = 1μm and W = 32 μm. Neglect the channel length modulation effect. **(07 Marks)**

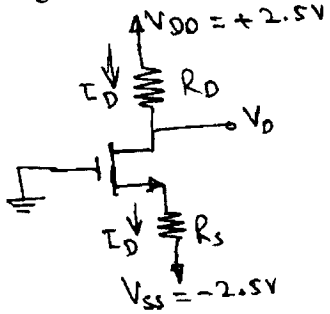

Fig.Q.2(c)

3 a. What is MOSFET scaling? Mention the benefits of scaling. **(06 Marks)**

b. Draw the MOSFET constant current source circuit and explain it. **(06 Marks)**

c. Explain the operation of a MOS current steering circuit and mention it advantage. **(08 Marks)**

4 a. What is cascade amplifier? Explain the operation of a MOS cascade amplifier. **(07 Marks)**

b. Draw the high frequency-equivalent circuit model of the MOSFET common source amplifier and explain the significance of each element. **(07 Marks)**

c. Draw the three different transistor pairings and explain each configuration. **(06 Marks)**

5 a. Explain the operation of MOS differential pair with a differential input voltage. **(07 Marks)**
b. Draw the circuit diagram of a active-loaded MOS differential pair and explain it. **(08 Marks)**
c. What are the features of two-stage CMOS op-amp configuration? **(05 Marks)**

PART – B

6 a. Explain the effect of feedback on the amplifier poles. **(06 Marks)**
b. What are the properties of negative feedbacks? Explain in detail. **(08 Marks)**
c. Draw the ideal structure for the series-series feedback amplifier and explain it. **(06 Marks)**

7 a. Explain how to minimize the temperature effect in a logarithmic amplifier. **(08 Marks)**
b. Draw the sample and hold circuit using op-amp and explain it. **(07 Marks)**
c. Design a non-inverting op-amp with a gain of 2. At the maximum output voltage of 10V and the current in the voltage divider is to be 10μA. **(05 Marks)**

8 a. What are the reasons for choosing CMOS over bipolar technology in digital applications? **(04 Marks)**
b. Explain the dynamic operation of a CMOS inverter. **(10 Marks)**
c. Implement $F = \overline{AB + CD}$ using the AOI gate. **(06 Marks)**

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Sixth Semester B.E. Degree Examination, June/July 2014
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a neat diagram, derive the expression for i_D in saturation and triode region. What happened to i_D if the channel length modulation is considered? **(10 Marks)**

b. Draw the large signal equivalent circuit model of NMOS and explain. **(04 Marks)**

c. Determine the voltages at all nodes and the currents through all the branches of following circuit. Let V_t = 1V and $kn'(W/L)$ = 1mA/V^2. Neglect the channel – length modulation effect. **(06 Marks)**

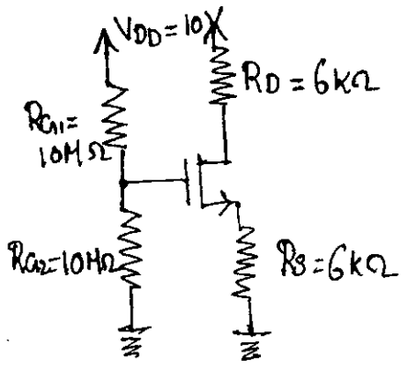

Fig.Q.1(c)

2 a. Show the development of the T equivalent – circuit model for the MOSFET from hybrid π model without channel length modulation. **(06 Marks)**

b. Draw the circuit of common-source amplifier with a source resistance. Draw its small signal equivalent circuit with γ_0 neglected. Obtain the expression for V_{gs}, id, v_o, A_v, A_{vo} and the overall voltage gain G_v. **(10 Marks)**

c. What is scaling? Differentiate constant field scaling and constant-voltage scaling. **(04 Marks)**

3 a. Briefly explain about short channel effect due to scaling. **(06 Marks)**

b. Compare NMOSFET and BJT in terms of
i) Current voltage characteristic.
ii) High frequency model.
iii) Output resistance. **(06 Marks)**

c. Following figure shoes the high frequency equivalent circuit of a common-source MOSFET amplifier. The amplifier is fed with a signal generator Vsig having a resistance Rsig. Resistance R in is due to the biasing network. Resistance R'_L is the parallel equivalent of the load resistance RL, the drain bias resistance R_D, and the FET output resistance ro. Capacitors cgs and cgd are the MOSFET internal capacitance:

i) Draw the equivalent circuit at midband frequencies.
ii) Draw the circuit for determining the resistance seen by Cgs.
iii) Draw the circuit for determining the resistance seen by Cgd. For Rsig = 100KΩ, Rin = 420KΩ, Cgs = Cgd = 1pF, gm = 4mA/V, and R'_L = 3.33KΩ
iv) Find the mid band voltage gain $A_M = V_0/Vsig$.
v) Find the upper 3-dB frequency f_H. **(08 Marks)**

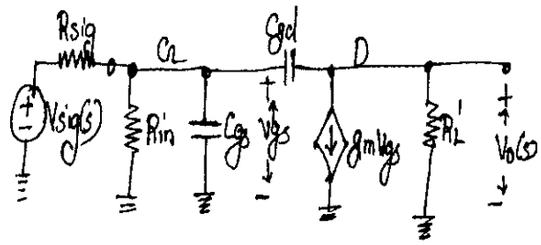

Fig.Q.3(c)

4 a. In common-gate amplifier with active load, obtain 3-dB frequency f_H using open circuit time constants. Draw the circuit required for determining Rgs and Rgd. **(08 Marks)**
b. Draw the $C_D - C_S$, $C_D - C_E$ and $C_D - C_a$ configurations. **(06 Marks)**
c. Draw an I_C source follower circuit. Obtain its small signal equivalent circuit and obtain its voltage gain $A_V = \frac{V_0}{V_i}$. **(06 Marks)**

PART – B

5 a. Obtain common-gate and common-mode rejection ratio (CMRR) of the MOS differential amplifier. Also find the effect of R_D mismatch on CMRR. **(12 Marks)**
b. Draw the two-stage CMOS op-amp configuration and briefly explain. Obtain overall dc open-loop gain. **(08 Marks)**

6 a. Briefly explain about
i) Voltage amplifier
ii) Current amplifier
iii) Trans conductance amplifier
iv) Trans resistance amplifier. **(08 Marks)**
b. Explain about series-shunt feedback amplifier with diagram and obtain the expression for input impedance and output impedance. **(08 Marks)**
c. Briefly explain about stability and pole locations. **(04 Marks)**

7 a. Draw and explain about weighted summer capable of implementing summing coefficients of both signs. **(06 Marks)**
b. Explain about DC imperfections. **(04 Marks)**
c. Write short notes on:
i) Antilogarithmic amplifiers.
ii) Analog multipliers. **(10 Marks)**

8 a. Draw the CMOS realization of A01 gate and explain with truth table. **(08 Marks)**
b. Draw and explain the exclusive OR function using PUN and PDN. **(08 Marks)**
c. What all are the parameters used to characterize the operation and performance of a logic circuit family. **(04 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, June/July 2015
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE questions, selecting THREE from Part-A and TWO from Part-B.***

PART – A

1 a. Derive the $i_D - V_{DS}$ relationship of a MOSFET for triode and saturation region. **(12 Marks)**

b. For a MOSFET process technology with W/L = 8 μm/0.8 μm, t_{ox} = 8nm, ϵ_r = 3.9 μ_h = 450 $cm^2/v.s$ and v_t = 0.7 V.

i) Find C_{ox} and K'_n.

ii) Calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_D = 100 μA.

iii) For the device to operate as a 1000 Ω resistor find the value of V_{GS} required for very small V_{DS}. **(08 Marks)**

2 a. Derive the expression for input resistance, output resistance, voltage gain and overall gain of a grounded source amplifier with a neat diagram. **(08 Marks)**

b. Design the biasing circuit shown in Fig.Q.2(b) to establish a drain current i_D = 0.5mA.

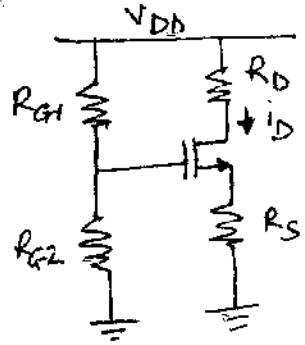

Fig.Q.2(b)

MOSFET has v_t = 1V, $k'_n(W/L) = 1\ mA/v^2$ and V_{DD} = 15V. Assume one-third V_{DD} across R_D and R_S and neglect channel length modulation λ = 0. Determine percentage change in value of i_D when MOSFET is replaced with another having v_t = 1.5V. **(12 Marks)**

3 a. Explain the operation of a MOSFET current steering circuits with necessary expressions. **(10 Marks)**

b. What is MOSFET scaling? Compare MOSFET parameters before and after scaling in constant field scaling and constant voltage scaling. **(10 Marks)**

4 a. Explain CMOS implementation of CS amplifier and arrive at voltage gain expression $A_v = g_{m1} r_{o1}/2$. **(10 Marks)**

b. Derive an expression for the short-circuit transconductance G_m of the MOS cascade amplifier. **(10 Marks)**

5 a. Explain operation of MOS differential pair with common-mode input voltage V_{cm} and determine the highest and lowest value of v_{cm} over which the differential pair operates properly. **(08 Marks)**

b. For a MOS differential pair in Fig.Q.5(b).

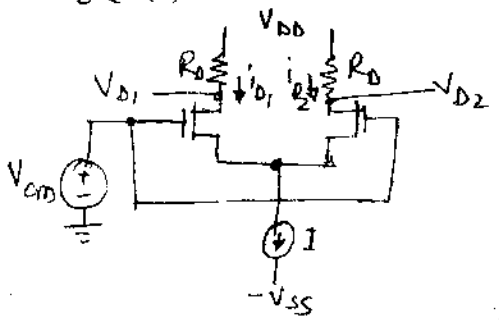

Fig.Q.5(b)

$V_{DD} = V_{SS} = 1.5V$, $k_n'(W/L) = 4mA/V^2$, $v_t = 0.5V$, $I = 0.4mA$, $R_D = 2.5\ K\Omega$ neglect channel length modulation.

i) Find V_{OV} and V_{GS} for each transistor.

ii) What is the highest value of V_{an} for Q_1 and Q_2 to remain in saturation?

iii) If the current source I requires a minimum voltage of 0.4V to operate properly what is the lowest value allowed for V_s and V_{an}? **(12 Marks)**

PART – B

6 a. Discuss with neat diagram the four basic feedback topologies. **(08 Marks)**

b. Explain the properties of negative feedback. **(08 Marks)**

c. What is the general structure of the feedback amplifier? **(04 Marks)**

7 a. Explain the operation and analysis of single op-amp difference amplifier to determine it common mode gain A_{cm}. **(10 Marks)**

b. How op-amp circuits can be used as signal integrator and differentiator and determine the time constants? **(10 Marks)**

8 a. Describe the circuit structure and static operation of CMOS invertor. **(08 Marks)**

b. With example explain PUN and PDN CMOS logic gate circuits. **(08 Marks)**

c. Realize two input NOR gate and two input NAND gate using CMOS gate. **(04 Marks)**

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Sixth Semester B.E. Degree Examination, June/July 2016
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting any Three from Part–A and Two from Part–B.***

PART – A

1 a. Derive the expression of $i_D - V_{DS}$ relationship for triode and saturation region of a NMOS transistor. **(10 Marks)**

b. For the MOSFET with $\frac{W}{L} = \frac{8\,\mu m}{0.8\,\mu m}$, calculate the values of V_{GS} and V_{DS}(min) needed to operate the transistor in the saturation region with a dc current $I_D = 100$. Assume $K'_n = 194\ \mu A/V^2$ and $V_t = 0.7$ V. **(05 Marks)**

c. Write the expression for the relationship between V_{SB} and V_t. Mention the effect of V_{SB} on the channel. **(05 Marks)**

2 a. What are the benefits of short channel MOSFETs? **(06 Marks)**

b. Explain the operation of a MOSFET current mirror. **(06 Marks)**

c. Draw the circuit of a MOS current steering circuit and explain it. **(08 Marks)**

3 a. Explain CMOS implementation of the common source amplifier and also draw its i-v characteristic of the active load and transfer characteristic. **(10 Marks)**

b. Consider a common gate amplifier specified as follows :
$\frac{W}{L} = \frac{7.2\mu m}{0.36\mu m}$. $\mu_n C_{OX} = 387\,\mu A/V^2$, $\gamma_0 = 18$ KΩ, $I_D = 100\ \mu A$, $g_m = 1.25$ mA/V, $\chi = 0.2$, $R_S = 10$ KΩ, $R_L = 100$ KΩ, $C_{gs} = 20$ fF, $C_{gd} = 5$ fF and $C_L = 0$. Find A_{VO}, R_{in}, R_{out}, G_V, G_{is}, G_i and f_H. **(10 Marks)**

4 a. What is cascade amplifier? Mention the basic idea behind it. **(04 Marks)**

b. Derive the expression of voltage gain and open circuit voltage gain of a IC-source follower. Draw its small signal equivalent circuit model. **(08 Marks)**

c. Explain the operation of a MOS differential pair with common-mode input voltage. **(08 Marks)**

5 a. Explain the operation of a two-stage CMOS op-amp configuration. Mention its features. **(10 Marks)**

b. Illustrate the method of differential to single-ended conversion. **(07 Marks)**

c. What are the factors contribute to the dc offset voltage of the MOS differential pair? **(03 Marks)**

PART – B

6 a. Discuss the properties of negative feedback in details. **(08 Marks)**

b. Explain the relationship between stability and pole location of an amplifier with effects. **(06 Marks)**

c. Draw the block diagram, representation of a series-shunt feedback amplifier and derive the expression of input resistance with feedback. **(06 Marks)**

7 a. Design a non-inverting amplifier with a gain of 2. At the maximum output voltage of 10 V and the current in the voltage divider is to be 10 μA. **(05 Marks)**

b. With a mathematical analysis and circuits, explain the temperature effects in Logarithmic amplifier are to be minimized. **(09 Marks)**

c. Draw the sample and hold circuit using op-amp and explain it. **(06 Marks)**

8 a. Define the following parameters of a logic circuit family and write the expressions :
i) Propagation delay.
ii) Robustness
iii) Delay-power product.
iv) Dynamic power dissipation. **(08 Marks)**

b. Implement :
i) $F = \overline{AB + CD}$ using the AND-OR-INVERT gate logic.
ii) $F = \overline{(A + B)(C + D)}$ using the OR-AND-INVERT gate logic. **(12 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, June/July 2017
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer Three questions from Part A and Two from Part B.***

PART – A

1 a. Draw the i_D-V_{DS} characteristics of a enhancement MOSFET. Indicate the all regions of operation and explain it. **(07 Marks)**

b. For the circuit shown in Fig. Q1 (b), derive the expression of voltage gain, overall voltage gain, input impedance and output impedence. **(10 Marks)**

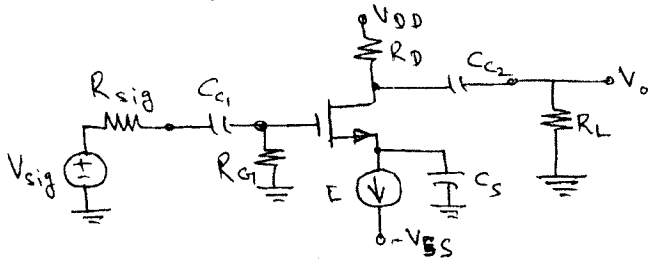

Fig. Q1 (b)

c. An nMOS transistor has $V_{to} = 0.8$ V, $2\phi_f = 0.7$V and $\gamma = 0.4\ V^{\frac{1}{2}}$. Find V_t when $V_{SB} = 3$ V **(03 Marks)**

2 a. The high frequency response an amplifier is characterized by the transfer function,

$$F_H(s) = \frac{1 - \frac{s}{10^5}}{\left(1 + \frac{s}{10^4}\right)\left(1 + \frac{s}{4 \times 10^5}\right)}$$. Determine the 3-dB frequency. **(04 Marks)**

b. Explain the operation of a current mirror using MOSFET. **(08 Marks)**

c. Draw the circuit diagram to generate a number of constant currents of various magnitudes using BJT and explain it. **(08 Marks)**

3 a. Draw the circuit of a common gate amplifier with active load and explain it. **(07 Marks)**

b. What is cascade amplifier? Mention the advantages of it. **(04 Marks)**

c. Consider a common gate amplifier specified as follows : $\frac{W}{L} = \frac{7.2\,\mu m}{0.36\,\mu m}$,

$\mu_n C_{OX} = 387\ \mu A/V^2$, $\gamma_0 = 18\,K\Omega$, $I_D = 100\ \mu A$, $g_m = 1.25\,mA/V$, $\psi = 0.2$, $R_S = 10\,K\Omega$, $R_L = 100K\Omega$, Cgs = 20fF, Cgd = 5 fF and $C_L = 0$. Find A_{VO}, R_{in}, R_{out}, G_V, G_{is} and G_i. **(09 Marks)**

4 a. Explain the operation of a MOS cascade amplifier. **(06 Marks)**

b. What is the need for transistor pairings? Draw all transistor pairings and mention advantages of each. **(08 Marks)**

c. Derive the expression of CMRR of a MOS differential amplifier for the two different cases. **(06 Marks)**

PART – B

5 a. Explain the operation of a active loaded MOS differential pair. **(08 Marks)**

b. Why differential amplifiers are well suited for IC fabrication? **(04 Marks)**

c. With neat circuit diagram, explain the operation of two-stage CMOS op-amp circuit. **(08 Marks)**

6 a. With a mathematical analysis, explain the effect of negative feedback on gain desensitivity and bandwidth extension. **(08 Marks)**

b. Draw the structure of a series-shunt feedback amplifier and derive the expression of input and output impedance with feedback. **(08 Marks)**

c. Draw the Root locus diagram for an amplifier with three poles and explain it. **(04 Marks)**

7 a. For the circuit shown in Fig. Q7 (a), determine the values of V_i, i_1, i_2, V_o and i_L. Also determine the voltage gain $\frac{V_0}{V_i}$, current gain $\frac{i_L}{i_i}$ and Power gain $\frac{P_0}{P_i}$. **(07 Marks)**

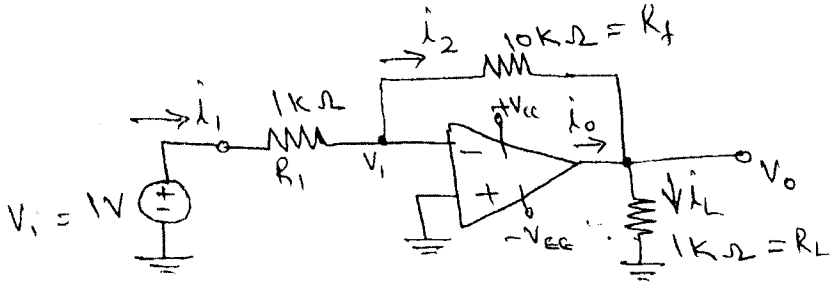

Fig. Q7 (a)

b. Derive the output voltage expression of a logarithmic amplifier with temperature compensation. **(09 Marks)**

c. With the help of waveform, explain the effect of slew rate limiting on output sinusoidal waveform. **(04 Marks)**

8 a. Define the following performance parameter of a logic circuit family and also draw the propagation delay and switching times waveform of the logic inverter.

(i) Noise margin

(ii) Propagation delay.

(iii) Robustness.

(iv) Delay-power product. **(10 Marks)**

b. Implement the following expressions using AOI gates and also write logic equivalent circuit

(i) $F = \overline{(A + B)(C + D)}$

(ii) $F = \overline{XY + \overline{Z}}$ **(10 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting at least TWO questions from each part.*
2. State all assumptions, including missing data.

PART – A

1 a. Derive an expression for drain-to-source current i_{DS} from i_D v/s V_{DS} relationship for triode and saturation regions of n-MOSFET. **(10 Marks)**

b. For an 0.8μm technology for which t_{OX} = 15nm, μ_n = 550 cm^2/V. Find k'_n and c_{OX} and the overdrive voltage $V_{ov} = V_{as} - V_t$ required to operate a transistor having W/L = 20 in saturation with I_D = 0.2 mA. What is the minimum V_{DS} needed? **(06 Marks)**

c. Design the circuit shown in Fig.Q.1(c) to obtain a drain voltage of 0.1V. What is the effective resistance between drain and source? At this operating point, let V_t = 0.8V and $K_n^1\left(\frac{W}{L}\right) = 1mA/V^2$. **(04 Marks)**

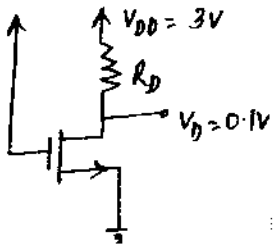

Fig.Q.1(c)

2 a. Briefly explain any two types of biasing methods in MOS amplifier circuits. **(06 Marks)**

b. For a common source amplifier with g_m = 2 mA/V, r_0 = 50KΩ and R_D = 10KΩ, R_G = 10MΩ, R_L = 20KΩ and R_{sig} = 0.5MΩ. Calculate R_{in}, G_v, A_v, A_{vo}, R_{out}. **(10 Marks)**

c. Mention any 4 comparison of important characteristics of MOSFET and the BJT. **(04 Marks)**

3 a. Explain the CMOS implementation of IC common source amplifier and hence explain how to determine its small signal voltage gain. **(10 Marks)**

b. For the common gate amplifier with W/L = 4μm/0.2μm, μ_nC_{OX} = 350 $\mu A/V^2$, r_0 = 18 KΩ, I_D = 100μA, g_m = 1.2 mA/V, χ = 0.2, R_s = 10KΩ, R_L = 100 KΩ, C_{gs} = 20fF, C_{gd} = 5fF, C_L = 5fF. Find A_{vo}, R_{in}, R_{out}, G_v, G_{is}, G_i and f_H. **(10 Marks)**

4 a. Explain the circuit of MOS cascade amplifier and hence obtain an expression for short circuit transconductance G_M. **(10 Marks)**

b. Explain briefly with neat circuit diagrams:
i) Wilson MOS mirror
ii) Widlar current source. **(10 Marks)**

PART – B

5 a. Explain the basic operation of BJT differential pair. **(08 Marks)**

b. For the nMOS differential pair with a common-mode voltage V_{cm} applied as shown in Fig.Q.5(b). let $V_{DD} = V_{SS} = 2.5V$, $K_n' W/L = 3mA/V^2$, $V_{tn} = 0.7V$, $I = 0.2mA$, $R_D = 5K\Omega$. Neglect channel length modulation.

i) Find V_{OV} and V_{GS} for each transistor.

ii) For $V_{CM} = 0$ find V_s, i_{D1}, i_{D2}, V_{D1} and V_{D2}.

iii) Repeat (ii) for $V_{cm} = 1V$.

iv) What is the highest value of V_{cm} for which Q_1 and Q_2 remain in saturation, if current source I requires a minimum voltage of 0.3V to operate properly. What is the lowest value for V_s and hence for V_{cm}. **(12 Marks)**

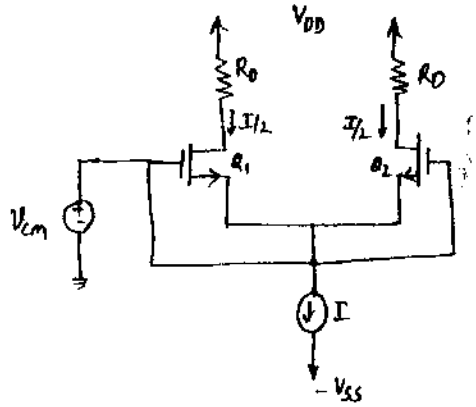

Fig.Q.5(b).

6 a. Explain briefly with expressions the properties of negative feedback. **(08 Marks)**

b. A series-shunt feedback amplifier employs a basic amplifier with input and output resistances each of 1KΩ and gain A = 2000 V/V. The feedback factor β = 0.1 V/V. Find the gain A_f the input resistance R_{i_f} and output resistance R_{o_f} of the closed loop amplifier. **(06 Marks)**

c. Explain briefly an alternative approach for finding loop gain Aβ. **(06 Marks)**

7 a. Explain instrumentation amplifier with neat circuit diagrams. **(08 Marks)**

b. With neat diagram, explain the sample and hold circuit using opamp. **(07 Marks)**

c. Derive an expression for an input resistance of the inverting amplifier taking into account the finite open loop gain A of the opamp shown in Fig.Q.7(c). **(05 Marks)**

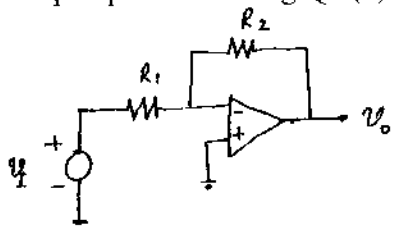

Fig.Q.7(c)

8 a. Briefly discuss the parameters used to characterize the operation and performance of logic circuit families. **(08 Marks)**

b. Write the expressions for propagation delay of an inverter. **(05 Marks)**

c. Sketch a CMOS logic circuit that realizes the function $Y = AB + \overline{AB}$ using equivalence or co-incidence function. **(07 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Dec.2014/Jan.2015
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

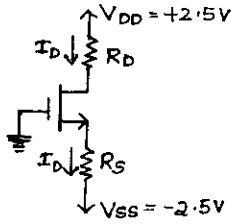
Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and TWO from Part-B.***

PART – A

1 a. Derive an expression for drain current of a MOSFET in different regions of operation. **(06 Marks)**

b. Design a circuit of Fig.Q.1(b), so that the transistor operates at $I_D = 0.4mA$ and $V_D = +0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\mu m$, and $W = 32\mu m$. Neglect channel length modulation effect ($\lambda = 0$). **(04 Marks)**

Fig.Q.1(b)



c. Draw the small signal circuit model of MOSFET when $|VSB| \neq 0$ and explain briefly. (ie including the body effect). **(04 Marks)**

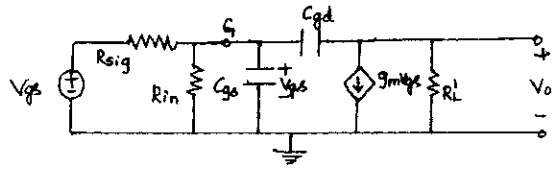
d. For the common drain amplifier stage, draw the small signal equivalent circuit and drive expressions for A_v, A_{vo}, G_v, R_{in} and R_{out}. **(06 Marks)**

2 a. Compare and explain the important characteristics of NMOS and NPN transistors. **(05 Marks)**

b. With a neat circuit diagram and equations explain the basic BJT current steering circuits. **(05 Marks)**

c. For the high frequency equivalent circuit of common source amplifier in Fig.Q.2(c), find the midband voltage gain $A_m = V_o/V_{sig}$ and upper 3dB frequency f_H using open circuit time constants. **(08 Marks)**

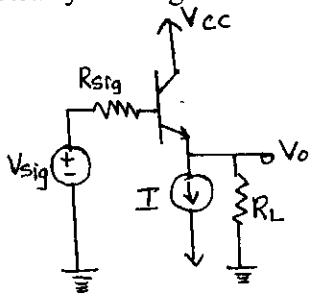
Fig.Q.2(c)



Where $R_L' = 3.3K\Omega$; $R_{sig} = 100K\Omega$; $R_{in} = 420K\Omega$; $C_{gs} = C_{gd} = 1Pf$, $g_m = 4m$ A/V.

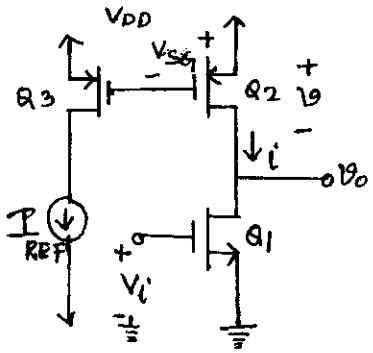
d. For the emitter follower biased by a constant current source I, shown in Fig.Q.2(d), draw the high frequency equivalent circuit clearly naming all the components: **(02 Marks)**

Fig.Q.2(d)



3 a. A CMOS common source amplifier shown in Fig.Q.3(a) is fabricated with W/L = 100 μm/1.6 μm for all transistors. With Kn′ = 90 μA/V², Kp1′ = 30 μA/V², IREF = 100μA, V_{An} = 8 V/μm and V_{AP} = 12 V/μm, determine the following quantities g_{m1}, r_{o1}, r_{o2}, A_{vo}. **(06 Marks)**

Fig.Q.3(a)



b. Draw the MOS cascade amplifier circuit with current source biasing. With the help of small signal equivalent circuit. Show that the cascading increases magnitude of open circuit voltage gain from A_o to A_o^2. **(06 Marks)**

c. Write short notes on cascade MOS current mirror circuit. **(04 Marks)**

d. Find A_o for an NMOS transistor fabricated in a 0.4μm CMOS process for which Kn′ = 200μA/V², and VA′ = 20V/μm. The transistor has a 0.4μm channel length and is operated with an overdrive voltage of 0.25V. What must be W for NMOS transistor to operate at I_D = 100μA? Also find r_o and g_m. **(04 Marks)**

4 a. Explain the operation of MOS differential pair with a differential input voltage and derive the range of differential input for differential mode of operation. **(08 Marks)**

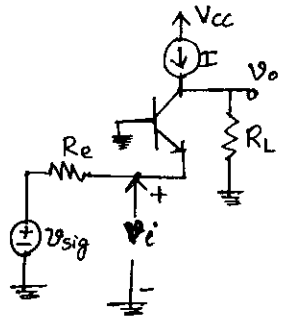
b. Prove that $A_{CM} = \frac{-r_{o4}}{2R_{SS}} \times \frac{1}{1+g_{m3}\,r_{03}}$ for the active loaded MOS differential amplifier. **(08 Marks)**

c. For the BJT differential amplifier having β = 100, matched to 10% or better, and areas that are matched to 10% or better, along with collector resistors that are matched to 2% or better, find V_{OS}, I_B and I_{OS}. The dc bias current is 100μA. **(04 Marks)**

5 a. Explain the operation of MOSFET as a linear amplifier. **(05 Marks)**

b. For the common base amplifier shown in Fig.Q.5(b) draw the small signal equivalent circuit and hence derive an expression for R_{in}, R_{out} and A_{vo}. **(06 Marks)**

Fig.Q.5(b)



c. A MOS differential amplifier is operated at a total current of 0.8mA, using transistors with W/L ratios of 100, $K_n' = \mu_n C_{ox}$ = 0.2 mA/V², V_A = 20V and R_D = 5KΩ. Find $V_{OV} = (V_{GS} - V_t)$, g_m, r_o, A_d. **(05 Marks)**

d. Explain channel length modulation effect of MOSFET. **(04 Marks)**

PART – B

6 a. What are the four properties of negative feed back? Briefly explain about each property. **(08 Marks)**

b. For the series-shunt feedback ideal amplifier find A_f, R_{if} and R_{of}. **(06 Marks)**

c. Discuss the method of frequency compensation for modifying open loop gain A(s) so that the closed loop amplifier is stable, by introducing a new pole in transfer function at sufficiently low frequency. **(06 Marks)**

7 a. Draw the circuit diagram of basic difference amplifier and derive an expression for the output voltage V_{out} and differential input resistance R_{id}. **(05 Marks)**

b. Show that the gain bandwidth product of an inverting amplifier is smaller than that of a non inverting amplifier. **(05 Marks)**

c. Find the output voltage of the circuit, assuming Op. Amp M1 has DC open loop gain of 1×10^5 and a bandwidth of 10 rad/sec., op amp M_2 is an ideal op. amp (Ref.Fig.Q.7(c)). **(06 Marks)**

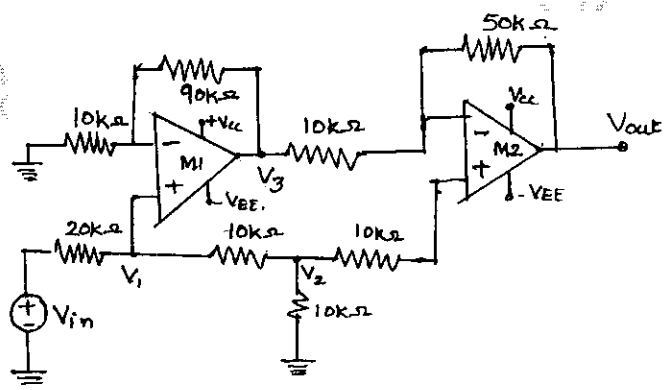


Fig.Q.7(c)

d. Write a note on use of op-amp in sample and hold circuit. **(04 Marks)**

8 a. Draw the basic structure of CMOS inverter and explain the voltage transfer characteristic of CMOS inverter **(08 Marks)**

b. Consider a CMOS inverter fabricated in a 0.25µm process for which C_{ox} = 6fF/µm^2, $\mu_n C_{ox} = 115\mu A/V^2$, $\pi_p C_{ox} = 30\mu A/V^2$, $V_{tn} = -V_{tp} = 0.4V$ and $V_{DD} = 2.5V$. The W/L ratio of Q_N is 0.375 µm/0.25µm and for Q_p is 1.125µm/0.25µm. The equivalent capacitance value is 6.25fF. Find t_{PHL}, t_{PLH} and t_p. **(06 Marks)**

c. Explain with neat circuit diagrams about pull-up and pull-down networks used in CMOS logic circuits. **(06 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Dec.2015/Jan.2016
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting THREE from PART-A and TWO from PART-B.***

PART – A

1 a. Explain channel length modulation effect and derive an expression for finite output resistance of a MOSFET in saturation region. **(08 Marks)**

b. Analyze the circuit shown in Fig. 1(b) to determine the voltages at all nodes and the currents through all branches let the nMOSFET $V_t = 1V$ and $k'_n \frac{W}{L} = 1mA/V^2$. Assume $\lambda = 0$. **(08 Marks)**

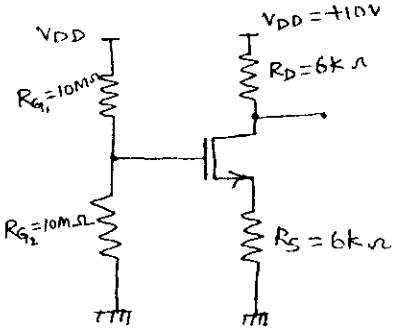

Fig.Q1(b)

c. Explain briefly biasing using constant current source. **(04 Marks)**

2 a. Derive analytical expressions for transfer characteristics of CS amplifier. **(08 Marks)**

b. Fig. Q2(b) shows a discrete CS MOSFET amplifier utilizing the drain to gate feedback biasing arrangement. Determine the small signal voltage. Gain its input resistance and the largest allowable input signal. Let $V_t = 1.5V$, $k'_n \frac{W}{L} = 0.25mA/V^2$ and $V_A = 50V$.

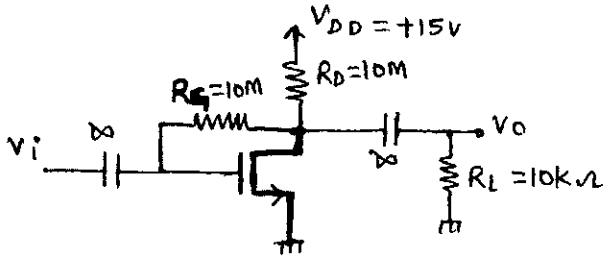

Fig.Q2(b) **(07 Marks)**

c. Briefly explain common drain amplifier. **(05 Marks)**

3 a. With neat circuit diagram, explain basic BJT current mirror and derive an expression for CT ratio of BJT current mirror for finite β. **(08 Marks)**

b. Derive an expression for 3dB frequency f_H for an amplifier having 2 poles and 2 zeros. **(08 Marks)**

c. Explain millers theorem. **(04 Marks)**

4 a. Briefly explain common source amplifier with active load. **(10 Marks)**

b. With neat circuit diagram, explain the MOS cascode amplifier. **(10 Marks)**

PART – B

5 a. Explain the operation of MOS differential pair with a common mode input voltage. **(07 Marks)**

b. Briefly explain the basic operation of BJT differential pair with neat circuit diagram. **(07 Marks)**

c. Explain two stage CMOS OPAMP. **(06 Marks)**

6 a. Write a note on gain desensitivity and bandwidth extension. **(06 Marks)**

b. Draw the ideal structure and equivalent circuit of the series shunt feedback amplifier and explain. **(10 Marks)**

c. Write a note on amplifier with a single pole response. **(04 Marks)**

7 A Derive an expression for the closed load gain (v_0/v_i) of the circuit shown in Fig. Q7(a). Assume the OPAMP is ideal. **(06 Marks)**

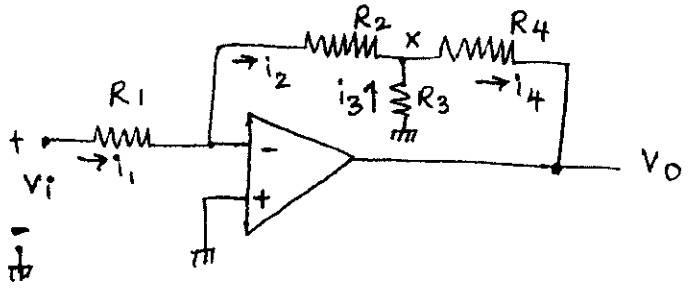

Fig.Q7(a)

b. Explain instrumentation amplifier with neat circuit diagram. **(08 Marks)**

c. With neat circuit diagram, explain antilog amplifier. **(06 Marks)**

8 a. A CMOS inverter fabricated in a 0.25 μm process has C_{ox} = 6 f F/μm^2, $\mu_n C_{ox}$ = 115 μA/v^2, $\mu_p C_{ox}$ = 30 μA, $v_{tn} = -v_{tp}$ = 0.4v and V_{DD} = 2.5v. The W/L ratio of Q_n is 0.375 μm/0.25μm, and that for Q_p is 1.125μm/0.25 μm. The gate – source and gate drain overlap capacitances are specified to be 0.3 f F/μm of gate width. Further the effective value of drain body capacitances are C_{dbn} = 1fF and C_{dbp} = 1 fF. The wiring capacitance C_W = 0.2f F. Find t_{PHL}, t_{PLH} and t_p. **(10 Marks)**

b. Implement $F = \overline{AB + \overline{AB}}$ using AOI. **(05 Marks)**

c. Explain two single input domino CMOS gate. **(05 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Micro Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the following parameters with respect to MOSFET:
i) Threshold voltage; ii) Overdrive voltage. **(05 Marks)**

b. Explain the breakdown effect occurs in MOSFET. **(05 Marks)**

c. Draw the biasing circuit using a drain to gate feedback resistor and explain it. **(05 Marks)**

d. For the circuit shown in Fig.Q.1(d), find the values of R and V_D to obtain a current I_D of 80μA. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $L = 0.8\ \mu m$ and $W = 4\ \mu m$. Assume $\lambda = 0$. **(05 Marks)**

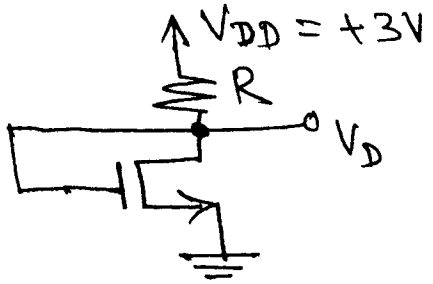

Fig.Q.1(d)

2 a. What are the disadvantages due to short-channel effects? **(05 Marks)**

b. The high frequency response of an amplifier is characterized by the TF

$$F_H(s) = \frac{1-\frac{s}{10^5}}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{4\times10^4}\right)}$$

. Determine the 3-dB frequency. **(05 Marks)**

c. What is current steering? Mention its advantages. **(05 Marks)**

d. Draw the circuit of basic MOSFET current source and explain it. **(05 Marks)**

3 a. Draw the circuit and small signal equivalent circuit of common source amplifier with active load and explain it. **(06 Marks)**

b. What is cascade amplifier and mention the basic idea behind the cascade amplifier? **(06 Marks)**

c. Draw the circuit of double cascading and explain it. **(08 Marks)**

4 a. Draw the transistor pairing circuits and mention the advantages of each pair. **(06 Marks)**

b. Draw the circuit of cascade MOS current mirror and explain it. **(06 Marks)**

c. Explain the operation of a MOS differential pair with a common mode input voltage and mention the relevant equations. **(08 Marks)**

PART – B

5 a. The differential amplifier shown in Fig.Q.5(a) uses transistors with $\beta = 100$. Evaluate:
   i) Input differential resistance (R_{id}).
   ii) Overall differential voltage gain V_o/V_{sig} (neglect the effect of V_o).
   iii) CMRR in dB. (Assume $A_{cm} = 5 \times 10^{-4}$).
   iv) Input common mode resistance (assuming that the early voltage $V_A = 100V$. **(10 Marks)**

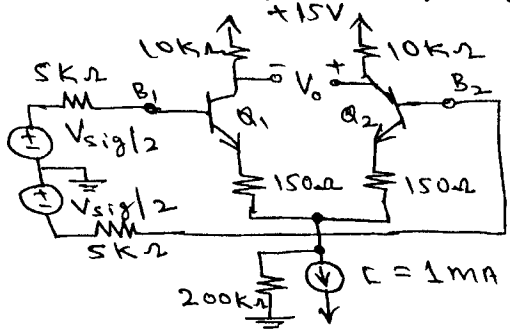

Fig.Q.5(a)

   b. Draw the two-stage CMOS Op-Amp circuit and explain it. **(10 Marks)**

6 a. Explain the properties of negative feedback. **(10 Marks)**
   b. Explain the effect of feedback on the amplifier stability and pole location. **(07 Marks)**
   c. What are the properties of current amplifier? **(03 Marks)**

7 a. Derive the expression for the closed loop gain V_o/V_{in} of the circuit shown in Fig.Q.7(a). **(08 Marks)**

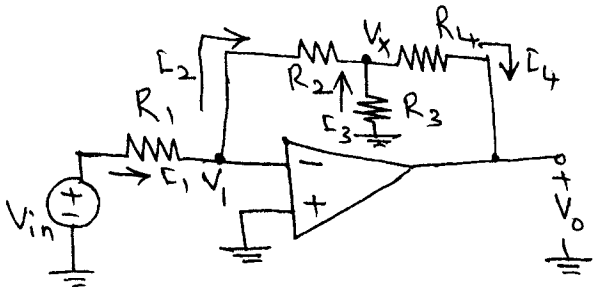

Fig.Q.7(a)

   b. With the help of mathematical analysis, explain how to minimize the temperature effect in logarithmic amplifier. **(10 Marks)**
   c. What are DC imperfections? **(02 Marks)**

8 a. Obtain the PUN from the PDN and vice versa for the following expressions:
   i) $Y = \overline{A(B+CD)}$ ii) $Y = \overline{A(B+AC)}$ **(12 Marks)**
   b. Define the following parameters with respect to CMOS:
   i) Propagation delay
   ii) Robustness
   iii) Delay power product
   iv) Dynamic power dissipation. **(08 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is channel length modulation? Derive the expression for finite output resistance of an NMOS transistor in saturation region. **(08 Marks)**

b. Calculate the value of r_{DS} obtained for a device having $K'_a = 100\,\mu A/V^2$ and W/L = 10 when operated with an overdrive voltage of 0.5V. Assume transistor is opening in triode region. **(04 Marks)**

c. Explain any three Biasing circuits in MOS amplifier. **(08 Marks)**

2 a. From the small signal operation of an amplifier, derive the expression for i) DC bias point ii) Signal current in the drain terminal iii) transconductance and iv) Voltage gain. **(08 Marks)**

b. A transistor amplifier is fed with a signal source having an open circuit voltage V_{sig} of 10mV and an internal resistance R_{sig} of 100kΩ. V_i and V_o are measured both without and with a load resistance R_L = 10kΩ connected to the amplifier output. The measured result are as follows :

	V_i (mv)	V_o (mv)
With R_L	8	70
Without R_L	9	90

Find: i) A_v ii) A_{vo} iii) G_v and iv) G_{vo}. **(04 Marks)**

c. With a neat circuit diagram and small signal model of common drain amplifier prove that $A_{vo} = 1$ and $G_v = 1$. **(08 Marks)**

3 a. For the high frequency equivalent circuit of a common source MOSFET amplifier shown in Fig. Q3(a) having R_{sig} = 100KΩ, R_{in} = 420KΩ, $C_{gs} = C_{gd}$ = 1pF, g_m = 4 MA/V and R'_L = 3.33KΩ. Find the midband voltage gain $A_m = \frac{V_o}{V_{sig}}$ and upper 3dB frequency.

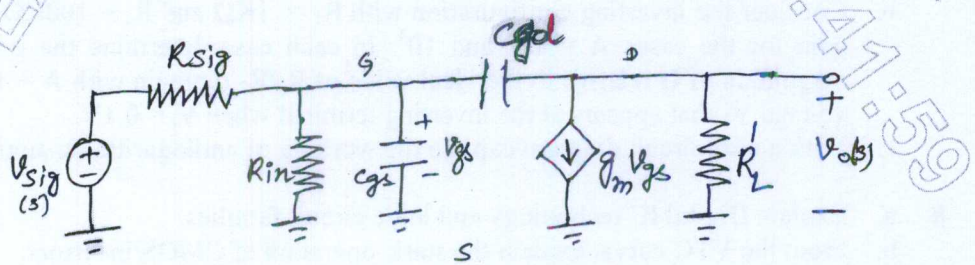

Fig Q3(a) **(08 Marks)**

b. What is scaling of MOSFET? Explain two types of scaling with examples. **(04 Marks)**

c. With a neat circuit diagram, explain the basic MOSFET current source and MOSFET current steering circuit. **(08 Marks)**

4 a. Derive the expression for R_{in}, G_{vo}, A_v and G_v of common gate amplifier with active load. **(10 Marks)**

b. Consider a CC-CE amplifier such that in Fig Q4(b) with the following specifications. $I_1 = I_2 = 1mA$, and identical transistors with $\beta = 100$, $f_T = 400MHz$ and $C_\mu = 2pF$. Let the amplifier be fed with a source V_{sig} having a resistance $R_{sig} = 4K\Omega$ and $r_e = 25m\Omega$. Assume a load resistance of $4K\Omega$, $g_m = 40mA/V$. Find the voltage gain A_m. **(10 Marks)**

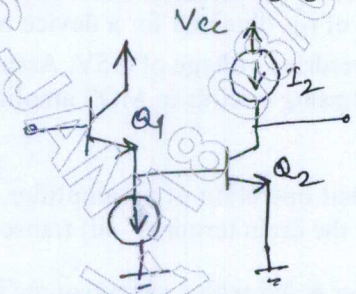

Fig Q 4(b)

PART – B

5 a. Derive the expression for common mode gain common mode rejection ratio of the MOS Differential amplifier. **(10 Marks)**

b. With a neat circuit diagrams explain the working of active loaded MOS Differential pair. **(10 Marks)**

6 a. With a neat block diagram, explain the General structure of feedback. **(08 Marks)**

b. Explain the effect of phase margin on closed loop response and hence prove that $|A_f(jw_1)| = \frac{1.3}{\beta}$. **(04 Marks)**

c. Explain the properties of Negative feedback. **(08 Marks)**

7 a. With neat circuit diagram, explain the working of instrumentation amplifier. **(08 Marks)**

b. Consider the inverting configuration with $R_1 = 1K\Omega$ and $R_2 = 100K\Omega$. Find the closed loop gain for the cases $A = 10^3$ and 10^4. In each case determine the percentage error in the magnitude of G relative to the ideal value of R_2/R_1 (contain with $A = \infty$) Also determine the voltage V_1 that appears at the inverting terminal when $V_i = 0.1V$. **(06 Marks)**

c. With a neat circuit diagram explain the working of antilogarithmic amplifier. **(06 Marks)**

8 a. Explain Digital IC technology and logic circuit families. **(08 Marks)**

b. From the VTC curve, explain the static operation of CMOS invertors. **(06 Marks)**

c. With example explain the working of CMOS logic gate circuit. **(06 Marks)**

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